RMx System On Module Specification

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CONTENTS

INTRODUCTION

This document details the physical and electrical interfaces for Blue Chip Technology 'RMx' System On Module (SOM) Products.

The RMx SOM product range is an ARM-based set of compact, processing modules designed for embedded control and media applications, and the host interfaces are designed to maximise re-use. A host platform designed for one SOM should be able to implement the same functionality using a different SOM with little or no adaptation.

COMPATIBILITY

Note that – unlike PC platform interface standards – System On Modules are designed to implement as much functionality as is practical 'on-card' (to keep host board design simple), and so it is not always possible or practical to use fully-standardised interfaces. As a few examples:-

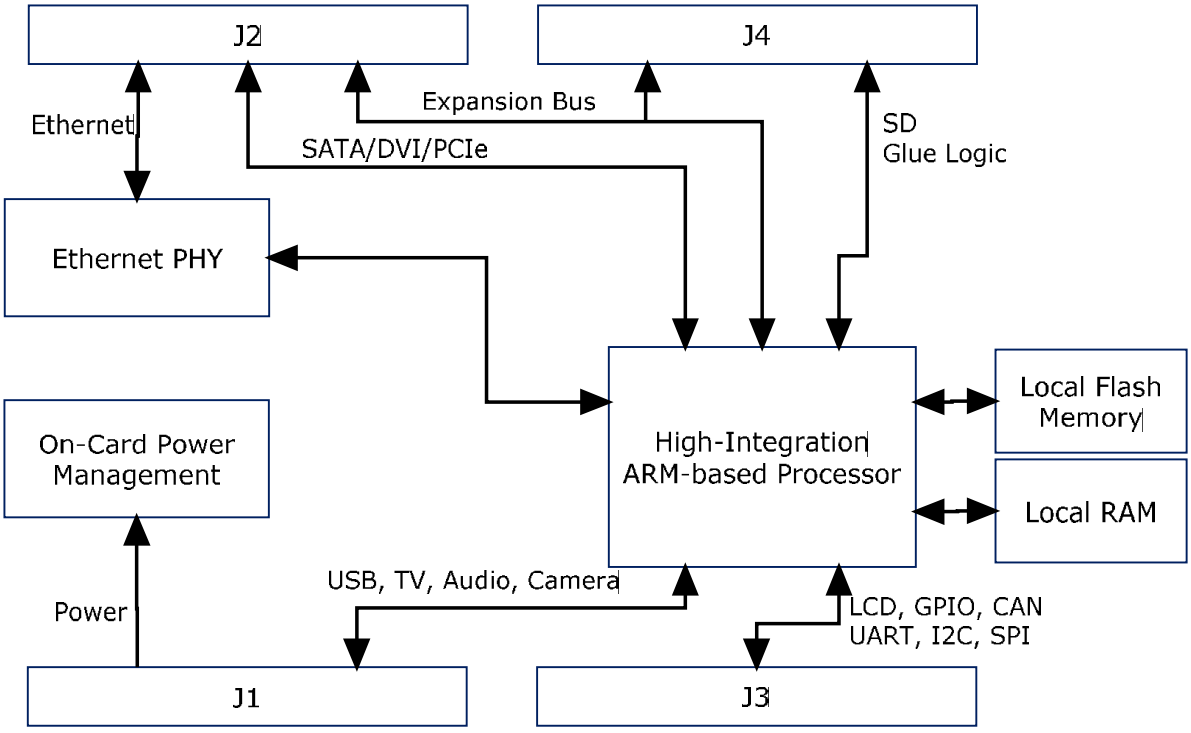
The SOM interface provides a basic wired Ethernet interface, which is implemented with the PHY on the SOM: this leaves the interface magnetics and final connector on the host board. Whilst it is possible to use the same magnetics with a range of PHY devices and accept the resulting trade-offs, it would be better to select a design which can offer a family of solutions in the same package so that a host board could be easily optimised for a range of PHY devices.

The SOM interface provides connections to enable extension of an on-card bus to enable devices on the host board to be close-coupled to the SOM processor. Whilst fairly simple devices can be supported from the SOM range, more complex implementations which are designed to take advantage of a particular processor may prove less tolerant of SOM changes. The host board designer has the option to either 'keep it simple' to improve cross-SOM compatibility, or tailor for a particular SOM/SOM family to gain a performance advantage or to enable functionality which couldn't otherwise be supported.

Interfaces and device mapping will always be a function of the main processing engine in use. Software should always abstract the main hardware layer in order to make porting between platforms easier.

MODULE OVERVIEW

The Blue Chip Technology RMx SOM is a compact module designed for use with a variety of carrier boards. It provides a rage of interfaces and functionality as indicated in the block diagram below. Actual interfaces and functionality varies with SOM module, but all use the same PCB header interconnect, and so suitably-designed carrier/host boards can work with a range of SOM modules.



SOM Block Diagram

INTERFACE PIN SUMMARY

In the following pin summaries, currently 'reserved' pins are greyed out. Host boards should not make connections to these pins without first consulting with Blue Chip Technology. Not all RMx SOM PCBs support all of the defined pins

J3

LCD	GND	2	1	GND	CAMERA
	LCD_D14	4	3	CAM_XD4	
	LCD_D15	6	5	CAM_XD5	
	GND	8	7	GND	
	LCD_D16	10	9	CAN_1	SLOW
	LCD_D17	12	11	CAN_2	SERIAL
	LCD_D18	14	13	CAN_3	
	LCD_D19	16	15	UARTA_TX	
	LCD_D20	18	17	UARTB_TX	
	LCD_D21	20	19	UARTA_ENTX	
	GND	22	21	UARTA_RX	
	LCD_D22	24	23	UARTB_RX	
	LCD_D23	26	25	GND	
	LCD_PCLK	28	27	SPI_CLK	
	GND	30	29	SPI_CSB	
	LCD_HSYNC	32	31	SPI_SIMO	
	LCD_VSYNC	34	33	SPI_SOMI	
	LCD_DE	36	35	SPI_CSA	
	LCD_D0	38	37	SOM_IRQA#	INTERRUPT
	LCD_D1	40	39	SOM_IRQB#	
	LCD_D2	42	41	GND	
	LCD_D3	44	43	I2CA_SCL	I2C
	GND	46	45	I2CA_SDA	
	LCD_D4	48	47	I2CB_SCL	
	LCD_D5	50	49	I2CB_SDA	
	LCD_D6	52	51	GPIO1	GPIO
	LCD_D7	54	53	GPIO2	
	LCD_D8	56	55	GPIO3	
	LCD_D9	58	57	GPIO4	
	GND	60	59	GND	
	LCD_D10	62	61	GPIO5	
	LCD_D11	64	63	GPIO6	
	LCD_D12	66	65	GPIO7	
	LCD_D13	68	67	GPIO8	
	GND	70	69	GND	

J1

LCD	LCD_ENA	2	1	GND	CAMERA
CNTRL	LCD_BL_ENA	4	3	CAM_XD3	
	GND	6	5	CAM_XD2	
USB	USB_HOST_P	8	7	CAM_XD1	
HOST	USB_HOST_N	10	9	CAM_XD0	
	GND	12	11	CAM_D9	
	USB_DEV_P	14	13	CAM_D8	
	USB_DEV_N	16	15	CAM_D7	
	GND	18	17	CAM_D6	
POWER	VCC5	20	19	GND	
	VIO	22	21	CAM_D5	
	VIO	24	23	CAM_D4	
TV	GND	26	25	CAM_D3	
	TV_LUMA_COMP	28	27	CAM_D2	
	GND	30	29	CAM_D1	
	TV_CHROMA	32	31	CAM_D0	
	GND	34	33	GND	
LCD	LCD_PWMB	36	35	CAM_STROBE	
PWM	LCD_PWMA	38	37	CAM_WEN	
	GND	40	39	CAM_FLD	
AUDIO	AUD_LINEIN_L	42	41	CAM_HS	
	AUD_LINEIN_R	44	43	CAM_VS	
	AUD_MICIN_BIAS	46	45	GND	
	AUD_MICIN_N	48	47	CAM_PCLK	
	AUD_MICIN_P	50	49	GND	
	GND	52	51	CAM_XCLKB	
	AUD_LINEOUT_R	54	53	CAM_XCLKA	
	AUD_LINEOUT_L	56	55	GND	
	GND	58	57	CAM_GLOBAL_RESET	
	IIS_DX	60	59	GND	
	IIS_DR	62	61	3V3_SBY	POWER
	IIS_CLKX	64	63	VCC3_3	
	IIS_FSX	66	65	VCC3_3	
	AUDIORSTN	68	67	VCC3_3	
	GND	70	69	VCC3_3	

J2

LAN	GND	2	1	GND	
	ETH_TX2_P	4	3	EXPN_CE0#	
	ETH_TX2_N	6	5	EXPN_CE1#	
	GND	8	7	GND	SATA
	ETH_RX2_P	10	9	SATA_RX_N	
	ETH_RX2_N	12	11	SATA_RX_P	
	GND	14	13	GND	
	ETH_TX1_P	16	15	SATA_TX_N	
	ETH_TX1_N	18	17	SATA_TX_P	
	GND	20	19	GND	DVI
	ETH_RX1_P	22	21	HDMI_C_N	
	ETH_RX1_N	24	23	HDMI_C_P	
	GND	26	25	GND	
	ETH_SPD_LED#	28	27	HDMI_D2_N	
	ETH_LNK_LED#	30	29	HDMI_D2_P	
	ETH_CTT	32	31	GND	
	GND	34	33	HDMI_D1_N	
BUS	EXPN_WP#	36	35	HDMI_D1_P	
EXPN	EXPN_CE4#	38	37	GND	
	EXPN_WE#	40	39	HDMI_D0_N	
	EXPN_RE#	42	41	HDMI_D0_P	
	EXPN_ALE	44	43	GND	
	EXPN_A11	46	45		
	EXPN_READY	48	47		
	EXPN_A7	50	49	GND	
	EXPN_A6	52	51	PCIE_CLK_P	PCIe
	EXPN_A5	54	53	PCIE_CLK_N	
	EXPN_A4	56	55	GND	
	EXPN_A3	58	57	PCIE_TX_P	
	EXPN_A2	60	59	PCIE_TX_N	
	EXPN_A1	62	61	GND	
	EXPN_D15	64	63	PCIE_RX_P	
	EXPN_D14	66	65	PCIE_RX_N	
	EXPN_D13	68	67	GND	
	GND	70	69	USB_DEV_VBUS	

J4

	GND	2	1	GND	
BUS	EXPN_FLASH_SEL	4	3		
EXPN	EXPN_D12	6	5		
[Continued]	EXPN_D11	8	7		
	EXPN_D10	10	9	GND	
	EXPN_D9	12	11		
	EXPN_D8	14	13		
	EXPN_D7	16	15		
	EXPN_D6	18	17		
	EXPN_D5	20	19		
	EXPN_D4	22	21	GND	
	EXPN_D3	24	23		
	EXPN_D2	26	25		
	EXPN_D1	28	27		
	EXPN_D0	30	29		
	GND	32	31	VCC3_3	
MISC	GPIO10	34	33	VCC3_3	
	PSON	36	35	VCC3_3	
	SYS_RESWARM#	38	37	VCC3_3	
	WAKEUP#	40	39	GND	
	EXPN_CLE	42	41	SD2_DATA0	SD/MMC
	BOOT_MODE#	44	43	SD2_DATA1	
	CAM_IRQ	46	45	SD2_DATA2	
	GPIO9	48	47	SD2_DATA3	
	SOM_IRQC#	50	49	SD2_CMD	
	WIRELESS_PWR_EN	52	51	SD2_CLK	
	EXPN_RESET#	54	53	GND	
	VBATT	56	55	VSD1	
	SD1_WP	58	57	SD1_CD	
	GND	60	59	SD1_DATA0	
	HDMI_HPD	62	61	SD1_DATA1	
	CEC	64	63	SD1_DATA2	
		66	65	SD1_DATA3	
	USB_OTG_ID	68	67	SD1_CMD	
	GND	70	69	SD1_CLK	

Note that the signal names used above are generic for all RMx modules. Each RMx module has an appendix including a description of how these generic signal names map onto the specific signal names used by each processor manufacturer.

SIGNAL/PIN DEFINITIONS

All directions are given with respect to the host/carrier board (ie: 'O' or 'Output' is a signal from the host board to the SOM).

[NB: See the latest revision for up-to-date listings of SOM units, and for allocations of any previously 'reserved'pins].

POWER

Power	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
VCC3_3	PWR	3.3V	Power feed for SOM	RM2/RM3
3V3_SBY	PWR	3.3V	Standby power feed for SOM	RM2/RM3
VIO	PWR	1.8V(typ) 3.3V (max)	Power reference from SOM	RM2/RM3
VCC5	PWR	5V	Power feed for SOM	RM2/RM3
VBATT	PWR	1.8V-3.3V	Nom 3V (1.8V-3.3V) DC power feed for SOM RTC	RM2/RM3
GND	PWR	0V	Power/signal ground	RM2/RM3

VIO is a reference supply provided by the RMx SOM to identify the configured logic level for a number of interfaces. For flexible support of RMx SOMs, this should be used to define the SOM side of a level-shifter for affected circuits. It is possible to operate without a level-shifter if a host platform is designed for a specific RMx SOM (in which case the I/O voltage can be designed against that provided in the specific RMx documentation).

It is recommended that host boards are able to support powering as in the table below to support the range of RMx SOMs anticipated. It is possible to reduce power levels based on the specific RMx modules targeted, but note that: a) figures are for the RMx only (additional power will be required for the host board and I/O interfaces; b) it is generally a good practice to allow a good margin on top of nominal figures to ensure power-up stability & reliability over life.

Provision of VBATT is optional (note that maintaining the RTC in power down may not be possible if this supply is not available). Typical drain in powered-off modes depends on implementation.

3V3_SBY is required, and should always be present whenever the other main supplies (VCC5 & VCC3_3) are available.

Example current levels

Rail:	*Nominal Voltage:*	*Current (RM2):*	*Current (RM3):*				*Recommended Supply:*
3V3_SBY	3.3V	0.1A	TBA				0.2A
VCC3_3	3.3V	1A	TBA				4A
VCC5	5V	0.1A	TBA				1A

LCD INTERFACE

Digital Display #1 (Parallel/LCD)	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
LCD_D0	I	VIO	24-bit parallel display interface	RM2/RM3
....LCD_D23	I			RM2/RM3
LCD_HSYNC	I		Horizontal synchronisation	RM2/RM3
LCD_VSYNC	I		Vertical synchronisation	RM2/RM3
LCD_PCLK	I			RM2/RM3
LCD_DE	I			RM2/RM3
LCD_ENA	I	VIO	Enable/disable panel	RM2/RM3
LCD_BL_ENA	I		Enable/disable backlight	RM2/RM3

PWM Output	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
LCD_PWMA	I	3.3V	Pulse-width modulator output	RM2/RM3
LCD_PWMB	I		Pulse-width modulator output	RM2/RM3

[If not required for brightness/contrast control, the PWM outputs can be used as general-purpose PWM outputs].

The LCD interface is designed for simple connection of panels offering a basic, parallel interface. Backlight/inverter power should be provided by the host PCB.

SLOW SERIAL INTERFACES

CAN	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
CAN_1	O	3.3V	RX (to SOM)	RM3
CAN_2	I		TX (from SOM)	RM3
CAN_3	I		TX_EN (from SOM)	RM3

The CAN transceiver is implemented on the host PCB when required.

UART A	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
UARTA_TX	I	3.3V	Serial transmit	RM2/RM3
UARTA_ENTX	I		Transmit enable control	RM2/RM3
UARTA_RX	O		Serial receive	RM2/RM3

UART B	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
UARTB_TX	I	3.3V	Serial transmit	RM2/RM3
UARTB_RX	O		Serial receive	RM2/RM3

Two, simple, two-wire UART interfaces are provided at basic logic level. UARTA adds a transmit enable signal to simplify use on multi-drop buses (eg: RS485) where disabling/tristating of the transceiver is required. Handshaking and access control, if desired, should be implemented at the software level (eg: using 'XON/XOFF').

UARTB is the default debug serial port. It is recommended that this be made available (as a minimum as contactable pads, or a pin header interface) on host boards.

SPI	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
SPI_CLK	I	3.3V		RM2/RM3
SPI_CSB	I			RM2/RM3
SPI_SIMO	I			RM2/RM3
SPI_SOMI	O			RM2/RM3
SPI_CSA	I			RM2/RM3

The Serial Peripheral Interface bus provided by the SOM operates with the SOM as master, and up to two slave addresses attached (selected using SPI_CSA & SPI_CSB) operating in independent mode. Note that – if two devices are used on this bus, both must be capable of operating in multi-slave environments (ie: must support 'slave select' signalling and tri-state outputs when not addressed).

I^2C INTERFACES

I^2C	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
I2CA_SCL	I/O	5V		RM2/RM3
I2CA_SDA	I/O	5V		RM2/RM3
I2CB_SCL	I/O	3.3V		RM2/RM3
I2CB_SDA	I/O	3.3V		RM2/RM3

I2CA is the default for use as a DDC channel for a display interface (see later).

GPIO

GPIO	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
GPIO1	I	3.3V	General purpose I/O signals	RM2/RM3
GPIO2	I			RM2/RM3
GPIO3	I			RM2/RM3
GPIO4	I			RM2/RM3
GPIO5	O			RM2/RM3
GPIO6	O			RM2/RM3
GPIO7	O			RM2/RM3
GPIO8	O			RM2/RM3
GPIO9	I		Often used for Bluetooth power enable.	RM2/RM3
GPIO10	O			RM3

The direction of each GPIO interface indicated above is supported by all RMx SOMs. Some RMx SOMs may offer more flexibility (see specific documentation for capabilities).

USB

USB Device	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
USB_DEV_P/N	I/O_{BAL}		Standard balanced USB bi-directional signal data bus	RM2/RM3
USB_DEV_VBUS	A	5V	Used to determine mode (*1)	RM2/RM3
USB_OTG_ID	O	5V	Standard USB OTG ID signal	RM3

[Note *1: The 'USB_DEV_VBUS' signal on the USB device interface is fed to the SOM to indicate presence of a suitable USB 'host' on the link].

The USB Device port is a principal interface for configuration of SOM modules. It is recommended that it be made available (at least as contactable pads, or a pin header) on host boards.

The “device” port may also support OTG functionality on some modules.

USB Host #1	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
USB_HOST_P/N	I/O_{BAL}		Standard balanced USB bi-directional signal data bus	RM2/RM3

TV

TV Display	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
TV_CHROMA	I_A		S-Video signals	RM2
TV_LUMA_COMP	I_A			RM2

TV out is not available on all RMx products.

AUDIO

Digital Audio	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
AUDIORSTN	I	VIO	Reset signal for host audio codecs	RM2/RM3[*1]
IIS_FSX	I	VIO	Framing for output channel	RM2/RM3[*1]
IIS_CLKX	I	VIO	Transmit/receive clock	RM2/RM3[*1]
IIS_DR	O	VIO	Receive data	RM2/RM3[*1]
IIS_DX	I	VIO	Transmit data	RM2/RM3[*1]

Analogue Audio	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
AUD_LINEOUT_L	I_A	3.3V	Left & right channel analogue signals	RM2/RM3[*1]
AUD_LINEOUT_R	I_A	3.3V		RM2/RM3[*1]
AUD_MICIN_P	O_A	3.3V	Balanced microphone analogue signal	RM2/RM3[*1]
AUD_MICIN_N	O_A	3.3V		RM2/RM3[*1]
AUD_MICIN_BIAS	I_A	3.3V		RM2/RM3[*1]
AUD_LINEIN_L	O_A	3.3V	Left line input (‘mono in’ for RM2)	RM2/RM3[*1]
AUD_LINEIN_R	O_A	3.3V	Right line input	RM3[*1]

Note *1: RM3 supports either digital or analogue audio. Selection is under software control. The ‘AUDIORSTN’ signal will be permanently active from RM3 whilst software selection is of the on-board codec (thus holding any host-board codec in hard-reset until it is enabled to avoid possible contention on the I2C & IIS buses).

The analogue audio channel provides signal levels typically up to 0dBu (0.775V rms).

AUD_MICIN_BIAS is a configurable, low-voltage bias voltage to power suitable microphones.

[Note that only a mono ‘line in’ channel is supported on RM2].

VIDEO/CAMERA INTERFACES

Digital Video In #1	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
CAM_GLOBAL_RESET	I	VIO		RM2/RM3
CAM_XCLKA	I	VIO		RM2
CAM_XCLKB	I	VIO		RM2
CAM_PCLK	O	VIO	Pixel clock	RM2/RM3
CAM_VS	O	VIO	Vertical Sync	RM2/RM3
CAM_HS	O	VIO	Horizontal Sync	RM2/RM3
CAM_FLD	O	VIO	Interleave frame indication	RM2
CAM_WEN	I	VIO	Enable camera function	RM2/RM3
CAM_STROBE	I	VIO	Controls camera light/flash	RM2/RM3
CAM_D0 - CAM_D9	O	VIO	10-bit parallel data	RM2/RM3
CAM_XD0 - CAM_XD1	O	VIO	Function depends on module	RM2/RM3
CAM_XD2 - CAM_XD5	O	VIO		RM3

The primary Digital Video Input #1 is designed for connection of cameras and similar devices to the SOM.

For maximum compatibility across modules it is recommended to use one of the following configurations:

- ITU-R BT.656 mode with 10-bit parallel data and embedded sync
- SYNC mode with 10-bit parallel data and separate Horizontal Sync and Vertical Sync

Other configurations are available, depending on which module is being used - see appendices for more information.

LAN/ETHERNET

Ethernet	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
ETH_SPD_LED#	I	3.3V	Open drain driver for “Speed” LED	RM2/RM3
ETH_LNK_LED#	I	3.3V	Open drain driver for “Link” LED	RM2/RM3
ETH_CTT	A		Centre-tap connection from magnetics	RM2/RM3
ETH_TX1_P/N	BAL		Transmit pair for 10/100Base-T	RM2/RM3
ETH_RX1_P/N	BAL		Receive pair for 10/100Base-T	RM2/RM3
ETH_TX2_P/N	BAL		Extra pairs for 1000Base-T	RM3
ETH_RX2_P/N	BAL			RM3

All SOMs support a basic 10/100Base-T Ethernet configuration; some support Gigabit Ethernet.

The PHY is implemented on the SOM; magnetics and connectorisation are required on the host board.

SATA

SATA	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
SATA_RX_P/N	O_{BAL}			RM3
SATA_TX_P/N	I_{BAL}			RM3

DVI/HDMI

Digital Display #2 (DVI/HDMI)	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
HDMI_C_P/N	I_{BAL}	3.3V	DVI-I (HDMI 1.4a support may also be available) interface	RM3
HDMI_D0_P/N	I_{BAL}			RM3
HDMI_D1_P/N	I_{BAL}			RM3
HDMI_D2_P/N	I_{BAL}			RM3
HDMI_HPD	O	3.3V	Hot Plug Detect signal from attached displays	RM3
CEC	I/O	3.3V	'Consumer Electronics Control' channel (for HDMI implementations)	RM3

Digital display #2 offers DVI-SL, and may optionally offer HDMI interface support[1].

If a DDC channel is required, I2CA should be used.

PCIE

PCI Express (x1)	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
PCIE_CLK_P/N	I_{BAL}	3.3V	Single-channel PCI express interface with reference clock (for any devices requiring this feature)	RM3
PCIE_TX_P/N	I_{BAL}			RM3
PCIE_RX_P/N	O_{BAL}			RM3

SDIO/SD/MMC

These ports provide connectivity to SD/MMC memory, or to SDIO devices (such as wireless modules).

SD/MMC/SDIO #1	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
SD1_WP	O	VSD1	Port for connection of flash memory devices or SDIO communication devices. VSD is a voltage output from the SOM to define and provide the I/O power for the interface. It can be also be turned off & on by the SOM to shutdown attached devices or provide a hard reset.	RM3
SD1_CD	O	3.3V		RM2/RM3
SD1_DATA0	I/O	VSD1		RM2/RM3
SD1_DATA1	I/O	VSD1		RM2/RM3
SD1_DATA2	I/O	VSD1		RM2/RM3
SD1_DATA3	I/O	VSD1		RM2/RM3
SD1_CMD	I/O	VSD1		RM2/RM3
SD1_CLK	I	VSD1		RM2/RM3
VSD1	A	[Note *1]		RM2/RM3

Note *1: VSD1 is sourced from the SOM and provides power for SD1-connected devices, and the reference voltage for any associated pull-up resistors. VSD1 is nominally in the range 2.7V to 3.6V or 1.7V to 1.95V. For maximum compatibility, use SD/SDIO or uSD cards able to operate in both voltage ranges.

[1] HDMI support may be subject to licensing

SD/MMC/SDIO #2	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
SD2_DATA0	I/O	3.3V	Port for connection of flash memory devices or SDIO communication devices. Note that voltage selection, card-detection, and write-protect features are not available for this interface	RM2/RM3
SD2_DATA1	I/O			RM2/RM3
SD2_DATA2	I/O			RM2/RM3
SD2_DATA3	I/O			RM2/RM3
SD2_CMD	I/O			RM2/RM3
SD2_CLK	I			RM2/RM3

Key Notes for Compatibility

SD1 is primarily designed for use with SD/MMC/SDIO devices. All RMx modules support 4-bit SD/SDIO/MMC cards operating at 'higher' voltage levels (typically 2.7V to 3.6V); not all RMx modules support switching to lower voltage mode (1.7V to 1.95V), but all support power cycling to enable card reset. Mechanical 'Write Protect' is not supported by all RMx cards.

SD2 is available for SD/MMC/SDIO type devices, but does not support any power control features or mechanical card detect/write protect. It is more appropriate for use as an interface to embedded devices on the host board.

For maximum compatibility, SD/SDIO or uSD devices are recommended.

The power supply should be decoupled at the card slot to minimise hot-insertion transients. Values of 47uF for SD cards, and 100uF for SDIO cards are recommended.

EXPANSION BUS

Expansion Bus	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
EXPN_A11	I	VIO		RM2/RM3
EXPN_A7	I			RM2/RM3
EXPN_A6	I			RM2/RM3
EXPN_A5	I			RM2/RM3
EXPN_A4	I			RM2/RM3
EXPN_A3	I			RM2/RM3
EXPN_A2	I			RM2/RM3
EXPN_A1	I			RM2/RM3
EXPN_D15	I/O		16-bit wide data bus	RM2/RM3
EXPN_D14	I/O			RM2/RM3
EXPN_D13	I/O			RM2/RM3
EXPN_D12	I/O			RM2/RM3
EXPN_D11	I/O			RM2/RM3
EXPN_D10	I/O			RM2/RM3
EXPN_D9	I/O			RM2/RM3
EXPN_D8	I/O			RM2/RM3
EXPN_D7	I/O			RM2/RM3
EXPN_D6	I/O			RM2/RM3
EXPN_D5	I/O			RM2/RM3
EXPN_D4	I/O			RM2/RM3
EXPN_D3	I/O			RM2/RM3
EXPN_D2	I/O			RM2/RM3
EXPN_D1	I/O			RM2/RM3
EXPN_D0	I/O			RM2/RM3
EXPN_CE0#	I		Three available chip-select signals. Note that some RMx modules may have restrictions on the use of these	RM2/RM3
EXPN_CE1#	I			RM2/RM3
EXPN_CE4#	I			RM2/RM3
EXPN_WP#	I		Write Protect	RM2

Expansion Bus	*Pin Type:*	*Power Rail /Tolerance:*	*Description:*	*Availability:*
EXPN_WE#	I		Data write strobe	RM2/RM3
EXPN_RE#	I		Data read strobe	RM2/RM3
EXPN_ALE	I		Address latch enable	RM2
EXPN_READY	I			RM2/RM3
EXPN_CLE	I		Command Latch Enable [NAND]	RM2
EXPN_RESET#	I		Can be used as a generic system reset	RM2/RM3

The expansion bus is provided as a flexible interface to memory-mapped host-board resources. The range available may vary dependent on RMx module in use, however there is some overlap in support.

Simple non-multiplexed devices (eg: suitably-configured FPGAs) with PSRAM/NOR flash like interfaces can be supported in order to implement specialised interface functionality.

MISCELLANEOUS

	Pin Type:	*Power Rail /Tolerance:*	*Description:*	*Availability:*
PSON	I	3.3V	Control wire from SOM 0 = Power off 1 = Power on	RM3
SYS_RESWARM#	O	[Use OD driver[2]]	Reset signal into SOM 0 = Reset RMx 1 = Normal operation	RM2/RM3
WAKEUP#	O	[Use OD driver]	'Wake' signal into SOM 0 = wake from sleep state 1 = [no change in state]	RM2/RM3
BOOT_MODE#	O	3.3V	[See below]	RM2/RM3
WIRELESS_PWR_EN3V	I	3.3V	Control wire from SOM 0 = Disable WLAN 1 = Enable WLAN	RM2/RM3
SOM_IRQA# SOM_IRQB# SOM_IRQC# CAM_IRQ	O O O O	VIO	Interrupt lines to SOM. 'CAM_IRQ' is dedicated to the primary digital video input. Pull up to VIO using 10K resistors on host board	RM2/RM3 RM2/RM3 RM2/RM3 RM2/RM3
EXPN_FLASH_SEL	O	5V 3.3V	[See below]	RM2 RM3

It is recommended that miscellaneous output pins should use open-drain drivers on the host, tolerant to 5V, in order to ensure full compatibility with all RMx modules. In practice, it is unlikely that these interfaces will be presented with more than 3.3V.

[2] Signal is pulled up on SOM (may be to any supply between 1.8V and 5V)

Use of 'BOOT_MODE#' and 'EXPN_FLASH_SEL' varies between RMx modules as indicated in the table below. These functions are intended for early development & product support purposes rather than for final product implementations.

Signal:	***Application:***	***Description:***
BOOT_MODE#	RM2	Normal (not connected): RMx boots from on-SOM Flash. Tied to GND: Changes the boot order to enable the module to attempt a boot from external peripherals before the on-SOM Flash memory
	RM3	Normal (not connected): RMx boot controlled by EXPN_FLASH_SEL. Tied to GND: Force boot from USB (serial loader)
EXPN_FLASH_SEL	RM2	Tied to GND: normal operation. The RMx boots from on-card Flash memory. The host board cannot make any connection to CS0 or CS1. Floating/pulled up: host board boot. Disables the on-SOM NAND Flash, freeing CS0 & CS1 for use on the host board. The boot NAND flash must be provisioned on the host board and connected to CS0.
	RM3	[Only effective if BOOT_MODE# is not connected] This pin is reserved for Blue Chip Technology use, and customers are advised to leave the pin floating (standard boot is from on-card Flash memory)

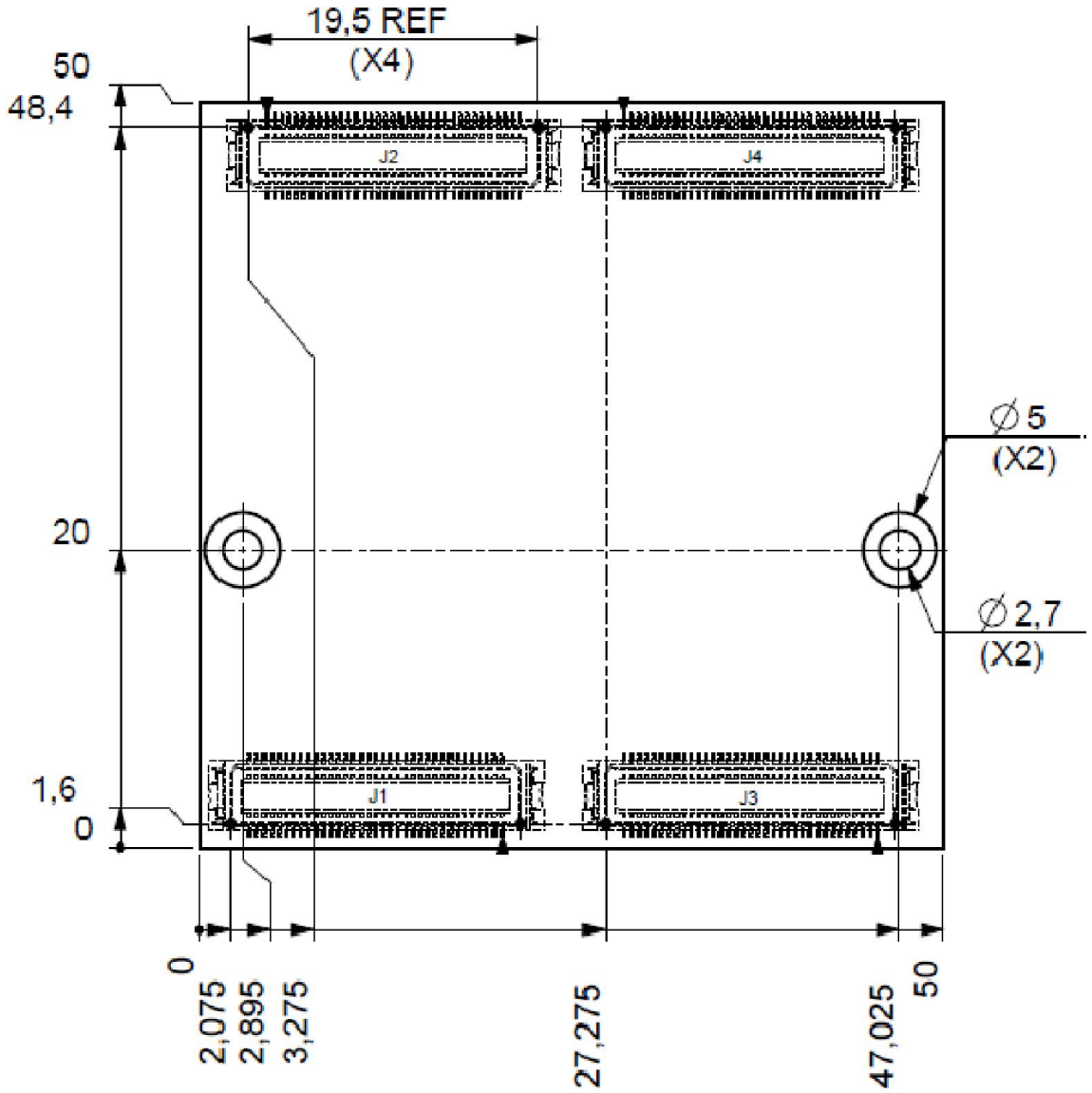
The above signals are pulled-up on the RMx (see the relevant Appendix for details), and so do not need to be pulled high on the host board in order to set a 'high' level.

BOOT_MODE# is a dual-purpose signal intended to enable:-

- Boot from alternative interface to enable initial program/re-program of the on-SOM Flash memory
- Entry into 'engineering mode' (depending on bootloader/operating system) to enable reconfiguration of operating modes of the SOM

The former is triggered if the signal is active at power-up; the latter function is reliant on using a suitable boot-loader, and is entered dependant on a software test of the same signal some time after initial power-up.

MECHANICAL SPECIFICATION



Notes:-

1. The above shows the position of the SOM mounting sockets and outline of the SOM module as seen from the top of the PCB/host board
2. Pin 1 position is 'rotational': it appears top-left of sockets J2 & J4 as shown, and bottom-right of sockets J1 & J3 sockets
3. Polarity is ensured by the difference in spacing of the LH & RH socket pairs: it is not possible to fit the PCB incorrectly
4. The SOM PCB is secured in place with two mount-pillars (shown)
5. The connectors on the SOM module are 70-pin Hirose DF17-3.0-70DS-0.5 connectors. The mating half required on the carrier board would be the Hirose DF17-XX-70DP-0.5 where XX can be 2.0 or 2.5 or 4.0 which specifies the stacking height adjustment. With the DF17-2.0-70DS-0.5 the baseboard adds 2mm to the SOM module's 3mm to create a 5mm stacking height (between PCBs). Similarly the DF17-2.5-70DS-0.5 will create a 5.5mm stacking height; the DF17-4.0-70DS-0.5 would create a 7mm stacking height

APPENDIX A – WORKING WITH RM2

The following section describes features of the SoM interface that are specific to the RM2 module.

The RM2 is based on the TI OMAP3 family of processors, including:

- AM3703 – Single core ARM Cortex-A8
- DM3730 – Single core ARM Cortex-A8 with DSP and 3D / video accelerators

When designing with RM2 you will need access to the appropriate processor data sheet & technical reference manual, which can be found at the TI web site:

http://www.ti.com/product/am3703

http://www.ti.com/product/dm3730

POWER

VIO is 1.8V on RM2. This means that level shifters may be required on the host board for any signals referenced to VIO.

LCD INTERFACE

The parallel LCD interface is based on the OMAP processor DSS interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	OMAP Processor Signal
LCD_D0 to LCD_D23	DSS_DATA0 to DSS_DATA23
LCD_HSYNC	DSS_HSYNC
LCD_VSYNC	DSS_VSYNC
LCD_PCLK	DSS_PCLK
LCD_DE	DSS_ACBIAS
LCD_ENA	GPIO_1
LCD_BL_ENA	GPIO_10

This interface is referenced to VIO, so it works at 1.8V logic levels on RM2.

There are also two PWM signals which can be used to control backlights etc.
On the RM2, these are open drain drivers that are intended for loads connected to a maximum of 3.3V. They can deliver considerable current:

SoM Signal	Current capability	Effective source resistance at max current
LCD_PWMA	Maximum 160mA	3R (typ) 4R (max)
LCD_PWMB	60mA	10R (typ) 12R (max)

However, it it recommended that these signals only be used for low-power control inputs to backlight power systems.

I²C INTERFACES

The I2C signals are pulled up on the RM2 with 10K. They should be pulled up on the host board with at least another 10K (making approx. 5K total). The optimum value for I2C pull-ups varies depending on bus capacitance, which is affected by the number of attached devices and the total bus length. Depending on your host board design, it may be necessary to reduce the host board pull-ups from 10K to 4K7 or 3K3.

There are four I2C buses available on the OMAP processor, but only two of these are available on the SoM connectors.

SoM Signals	OMAP Processor Signals	Comments
I2CA_SCL, I2CA_SDA	I2C2_SCL, I2C2_SDA	5V bus
I2CB_SCL, I2CB_SDA	I2C3_SCL, I2C3_SDA	3V3 bus

RM2 does not have any devices on these buses, so all addresses are available for devices on the host board.

GPIO

The GPIO signals on RM2 are buffered, so their electrical characteristics are determined by the buffer (SN74AVC32T245), not the processor. A link to the datasheet is provided below:

http://www.ti.com/lit/ds/sces553e/sces553e.pdf

USB

The USB lines for device and host are balanced differential pairs. The recommendation is to use a characteristic impedance of 90R +/- 15% for tracking. The USB Implementers Forum has this advice:

> Use 30 ohms to ground, 90 ohms differential between the USB data lines. Be aware that many differential impedance formulas don't take into account the presence of a plane next to the data lines and tend to overestimate the reduction in single-ended impedance due to coupling between the two lines. For typical buried microstrips on spacings FR4 stackups the USB traces should be somewhere around 11 or 12mils wide with roughly a 33mil edge to edge spacing (45mils center to center). This is far enough apart that there's almost no coupling between the lines---the single-ended impedance is around 1.5O lower than what a single trace's impedance would be.

It is recommended to keep each signal in the differential pair the same length to within 2.5mm.

TV

RM2 supports a TV output with S-Video (luma + chroma) signals, based on the OMAP 3 Video Encoder block. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	OMAP Processor Signal
TV_LUMA	CVIDEO1_OUT
TV_CHROMA	CVIDEO2_OUT

Both signals are high-frequency and noise sensitive. Tracking should be as short as possible, and with a characteristic impedance of 75Ω. The two signal traces should be closely matched (recommend routing together) and kept away from other possible interfering signals as far as possible.

AUDIO

The digital audio interface is based on the OMAP processor MCBSP2 interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	OMAP Processor Signal
IIS_FSX	MCBSP2_FSX
IIS_CLKX	MCBSP2_CLKX
IIS_DR	MCBSP2_DR
IIS_DX	MCBSP2_DX
AUDIORSTN	GPIO_59 (open drain, pulled up to VIO=1V8)

This interface is referenced to VIO, so it works at 1.8V logic levels on RM2.

Note that AUDIORSTN is connected to GPMC_RESET# and when driven low, will also reset the Ethernet PHY on the RM2. It is recommended not to drive this line from the host board when using RM2.

The analogue audio interface has the following characteristics:

Analogue Audio Parameter	Value
Mic/Line In Impedance	40K (min) 70K (max)
Mic/Line In Voltage	1.5V pk-pk (max)
Mic/Line In THD	-75dB @ 1kHz, 0dBFs
Line Out Impedance	10K (min)
Line Out Voltage	1.5V pk-pk (0dBFs)
Line Out THD	-75dB @ 1kHz, 0dBFs
Mic Bias Voltage	2.2V (typ)
Mic Bias Load Current	1mA (max)
Mic Bias Internal Resistance	60K (typ) 70K(max)

VIDEO / CAMERA INTERFACE

The digital video interface is based on the OMAP processor CPI (Camera Parallel Interface) block.
The processor signal names and SoM generic signal names are the same, except as shown below:

SoM Signal	OMAP Processor Signal
CAM_XD0	CAM_D10
CAM_XD1	CAM_D11

This interface is referenced to VIO, so it works at 1.8V logic levels on RM2.

Supported configurations include:

Data bus format	Data bus pins used	Mode
8-bit parallel	CAM_D0 - CAM_D7	SYNC
10-bit parallel*	CAM_D0 - CAM_D9*	SYNC*
11-bit parallel	CAM_D0 - CAM_D9, CAM_XD0	SYNC
12-bit parallel	CAM_D0 - CAM_D9, CAM_XD0 - CAM_XD1	SYNC
8-bit parallel	CAM_D0 - CAM_D7	ITU-R BT.656
10-bit parallel*	CAM_D0 - CAM_D9*	ITU-R BT.656*
Single lane serial	CAM_D0 - CAM_D1	MIPI CSI2
Two lane serial	CAM_D6 - CAM_D9	MIPI CSI2

*These configurations are recommended for maximum compatibility with other modules

For more details, see the processor Technical Reference Manual.

LAN / ETHERNET

This is a standard interface. The data signals are terminated with 49.9R on the RM2 module, and should be routed as differential pairs with a differential impedance of 100R.

When using an RJ45 connector, the following points should be noted:

1. The centre tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75R resistor through a 1000 pF, 2KV capacitor to chassis ground.
2. The centre tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75R resistor through a 1000 pF, 2KV capacitor to chassis ground.
3. Only one 1000 pF, 2KV capacitor to chassis ground is required. It is shared by both TX & RX centre taps.

The mapping between RJ45 pins and SoM generic signal names is shown below:

SoM Signal	RJ45 pin
ETH_TX1_P	1
ETH_TX1_N	2
ETH_RX1_P	3
ETH_RX1_N	6

The LED drivers are open drain, and are intended to drive LEDs attached to a maximum of 5.5V
The LED drivers can provide up to 4mA

SDIO/SD/MMC

The SD1 interface is based on the OMAP processor MMC1 interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	OMAP Processor Signal
SD1_CD	GPIO0 (on TPS65930)
SD1_DATA0	MMC1_DAT0
SD1_DATA1	MMC1_DAT1
SD1_DATA2	MMC1_DAT2
SD1_DATA3	MMC1_DAT3
SD1_CMD	MMC1_CMD
SD1_CLK	MMC1_CLK
SD1_WP	Not supported on RM2

This interface is referenced to VSD, so it works at 1.8V or 3.3V logic levels. (SD cards start communicating at 3.3V when inserted, but may subsequently negotiate with the cpu to work at 1.8V instead.)

The SD2 interface is based on the OMAP processor MMC2 interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	OMAP Processor Signal
SD2_DATA0	MMC2_DAT0
SD2_DATA1	MMC2_DAT1
SD2_DATA2	MMC2_DAT2
SD2_DATA3	MMC2_DAT3
SD2_CMD	MMC2_CMD
SD2_CLK	MMC2_CLK

This interface works at 3.3V logic levels only.

EXPANSION BUS

The Expansion bus is based on the OMAP processor GPMC interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	OMAP Processor Signal
EXPN_D0 to EXPN_D15	GPMC_D0 to GPMC_D15
EXPN_A1 to EXPN_A7	GPMC_A1 to GPMC_A7
EXPN_A11	GPMC_A10
EXPN_CE0# EXPN_CE1# EXPN_CE4#	GPMC_nCS0 GPMC_nCS3 GPMC_nCS4
EXPN_WP#	GPMC_nWP
EXPN_WE#	GPMC_nWE
EXPN_RE#	GPMC_nOE
EXPN_ALE	GPMC_nADV_ALE
EXPN_READY	GPMC_WAIT0
EXPN_CLE	GPMC_nBE0_CLE
EXPN_RESET#	GPIO_59

This interface is referenced to VIO, so it works at 1.8V on RM2.

EXPN_CE0#, EXPN_CE1#, EXPN_CE4# are each pulled up to the 1.8V rail with 10K.

EXPN_CE0# and EXPN_CE1# are both used for the on-board Flash. They can be used for other devices only if the on-board Flash is disabled using EXPN_FLASH_SEL.

MISCELLANEOUS

The miscellaneous signals are based on various OMAP interfaces. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	OMAP Processor Signal
SYS_RESWARM#	SYS_nRESWARM
WAKEUP#	SYS_OFFMODE (optional)
BOOT_MODE#	SYS_BOOT5 (after inversion)
EXPN_FLASH_SEL	Not directly connected
WIRELESS_PWR_EN	GPIO_41
SOM_IRQA# SOM_IRQB# SOM_IRQC# CAM_IRQ	GPIO_61 GPIO_170 GPIO_151 GPIO_65

SYS_RESWARM# is also connected to NRESWARM on the TPS65930, and is pulled up to VIO (1.8V) through 4K7.

WAKEUP# is also connected to NSLEEP1 on the TPS65930. WAKEUP# is not supported on standard RM2 modules, but can be offered as an option.

BOOT_MODE# is inverted before connection to SYS_BOOT5.

EXPN_FLASH_SEL is a special signal that is pulled up to 5V through 10K. It should be tied to Ground on the host board in order to enable the RM2 on-board Flash. Otherwise it can be left floating, in which case the RM2 on-board Flash is disabled, and the RM2 will boot from another peripheral or from Flash on the host board.

SOM_IRQB# and CAM_IRQ are each pulled up to VIO (1.8V) through 10K. It is recommended that all other interrupts are pulled up on the host board to ensure stable levels during start-up.

[NB: Whilst the interrupt lines are typically recommended to be active low or rising-edge triggered, it is possible for software to configure them to operate in other modes if required].

WIRELESS_PWR_EN is intended for use with SDIO WiFi cards on the host board. As well as being used for enabling power to the SDIO card, the signal emulates a “card detect” status within the RM2.

APPENDIX B – WORKING WITH RM3

The following section describes features of the SoM interface that are specific to the RM3 module.

The RM3 is based on the Freescale i.MX6 family of processors, including:

- i.MX6Q – Quad core ARM Cortex-A9 with 3D / 2D / video accelerators
- i.MX6D – Dual core ARM Cortex-A9 with 3D / 2D / video accelerators

When designing with RM3 you will need access to the appropriate processor data sheet & technical reference manual, which can be found at the Freescale web site:

http://www.freescale.com/webapp/sps/site/taxonomy.jsp?code=IMX6X_SERIES

POWER

VIO is 3.3V on RM3, and there are no signals that work at 1.8V logic levels.

LCD INTERFACE

The parallel LCD interface is based on the i.MX6 processor DI0 and DISP0 interfaces from the IPU block. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
LCD_D0 to LCD_D23	DISP0_DAT0 to DISP0_DAT23
LCD_HSYNC	DI0_PIN2
LCD_VSYNC	DI0_PIN3
LCD_PCLK	DI0_DISP_CLK
LCD_DE	DI0_PIN15
LCD_ENA	DI0_PIN4 (configured as gpio4 [20])
LCD_BL_ENA	GPIO_3

This interface is referenced to VIO, so it works at 3.3V logic levels on RM3.

There are also two PWM signals which can be used to control backlights etc.
On the RM3, these are logic signals capable of sourcing/sinking around 1mA and therefore can not be used to drive backlights directly, but are intended as PWM control inputs to a backlight driver.

SoM Signal	i.MX6 Processor Signal
LCD_PWMA	SD4_DAT1 (configured as pwm3 PWMO)
LCD_PWMB	SD4_DAT2 (configured as pwm4 PWMO)

I²C INTERFACES

The I2C signals are pulled up on the RM3 with 10K. They should be pulled up on the host board with at least another 10K (making approx. 5K total). The optimum value for I2C pull-ups varies depending on bus capacitance, which is affected by the number of attached devices and the total bus length. Depending on your host board design, it may be necessary to reduce the host board pull-ups from 10K to 4K7 or 3K3.

There are three I2C buses available on the i.MX6 processor, but only two of these are available on the SoM connectors.

SoM Signals	i.MX6 Processor Signals	Comments
I2CA_SCL I2CA_SDA	KEY_COL3 (configured as i2c2 SCL) KEY_ROW3 (configured as i2c2 SDA)	5V bus
I2CB_SCL I2CB_SDA	GPIO_5 (configured as i2c3 SCL) GPIO_16 (configured as i2c3 SDA)	3V3 bus

RM3 has the audio codec on bus B, so address 0x18 is taken and cannot be used for devices on the host board.

RM3 has the power management chip on bus A, so address 0x08 cannot be used for devices on the host board.

GPIO

The GPIO signals on RM3 are wired directly to the processor, and are fully configurable (e.g. input / output / open drain / pull-up / pull-down etc.).

SoM Signal	i.MX6 Processor Signal	
GPIO1	GPIO_4	
GPIO2	KEY_COL2	(configured as gpio4 [10])
GPIO3	ENET_CRS_DV	(configured as gpio1 [25])
GPIO4	ENET_TX_EN	(configured as gpio1 [28])
GPIO5	ENET_RXD0	(configured as gpio1 [27])
GPIO6	ENET_RXD1	(configured as gpio1 [26])
GPIO7	ENET_TXD0	(configured as gpio1 [30])
GPIO8	ENET_TXD1	(configured as gpio1 [29])
GPIO9	SD4_DAT4	(configured as gpio2 [12])
GPIO10	GPIO_6	

USB

The USB lines for device and host are balanced differential pairs. The recommendation is to use a characteristic impedance of 90R +/- 15% for tracking. The USB Implementers Forum has this advice:

> Use 30 ohms to ground, 90 ohms differential between the USB data lines. Be aware that many differential impedance formulas don't take into account the presence of a plane next to the data lines and tend to overestimate the reduction in single-ended impedance due to coupling between the two lines. For typical buried microstrips on spacings FR4 stackups the USB traces should be somewhere around 11 or 12mils wide with roughly a 33mil edge to edge spacing (45mils center to center). This is far enough apart that there's almost no coupling between the lines---the single-ended impedance is around 1.5O lower than what a single trace's impedance would be.

It is recommended to keep each signal in the differential pair the same length to within 2.5mm.

The USB_OTG_ID signal is attached to a i.MX6 input pin (ENET_RX_ER configured as OTG_ID).

AUDIO

The digital audio interface is based on the i.MX6 processor MCBSP2 interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
IIS_FSX	KEY_COL1 (configured as AUD5_TXFS)
IIS_CLKX	KEY_COL0 (configured as AUD5_TXC)
IIS_DR	KEY_ROW1 (configured as AUD5_RXD)
IIS_DX	KEY_ROW0 (configured as AUD5_TXD)
AUDIORSTN	SD4_DAT0 (configured as gpio2 [8]) gated with SD4_DAT6 (configured as gpio2 [14])

Note that AUDIORSTN is driven by a logic gate on RM3 and should not be driven by the host board.

This interface is referenced to VIO, so it works at 3.3V logic levels on RM3.

The analogue audio interface has the following characteristics:

Analogue Audio Parameter	Value
Mic/Line In Impedance	20K (min) 80K (max)
Mic/Line In Voltage	0.707V rms (max)
Mic/Line In THD	-75dB @ 1kHz, 0dBFs
Line Out Impedance	16R (min)
Line Out Voltage	0.707V rms (0dBFs)
Line Out THD	-65dB @ 1kHz, 0dBFs
Mic Bias Voltage	2V or 2.5V (configurable)
Mic Bias Load Current	4mA (typ)

VIDEO / CAMERA INTERFACE

The digital video interface is based on the i.MX6 processor CSI 0 (Camera Sensor Interface) block. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
CAM_D0 - CAM_D9	CSI0_DAT10 - CSI0_DAT19
CAM_XD0 - CAM_XD5	CSI0_DAT4 - CSI0_DAT9
CAM_GLOBAL_RESET	NANDF_CS2 (configured as gpio6 [15])
CAM_PCLK	CSI0_PIXCLK
CAM_VS	CSI0_VSYNC
CAM_HS	CSI0_MCLK (configured as ipu1 CSI0_HSYNC)
CAM_WEN	CSI0_DATA_EN

This interface is referenced to VIO, so it works at 3.3V logic levels on RM3.

Supported configurations include:

Data bus format	Data bus pins used	Mode
8-bit parallel	CAM_D2 - CAM_D9	SYNC
10-bit parallel*	CAM_D0 - CAM_D9*	SYNC*
11-bit parallel	CAM_D0 - CAM_D9, CAM_XD5	SYNC
12-bit parallel	CAM_D0 - CAM_D9, CAM_XD4 - CAM_XD5	SYNC
16-bit parallel	CAM_D0 - CAM_D9, CAM_XD0 - CAM_XD5	SYNC
8-bit parallel	CAM_D2 - CAM_D9	ITU-R BT.656
10-bit parallel*	CAM_D0 - CAM_D9*	ITU-R BT.656*
16-bit parallel	CAM_D0 - CAM_D9, CAM_XD0 - CAM_XD5	ITU-R BT.1120

*These configurations are recommended for maximum compatibility with other modules

For more details, see the i.MX6 Reference Manual.

LAN / ETHERNET

This is a standard interface. The data signals are terminated on the RM3 module, and should be routed as differential pairs with a differential impedance of 100R.

When using an RJ45 connector, the following points should be noted:

1. The centre tap connection on the cable side (RJ45 side) for the each data pair should be terminated with a 75R resistor through a 1000 pF, 2KV capacitor to chassis ground.
2. Only one 1000 pF, 2KV capacitor to chassis ground is required. It is shared by all centre taps.

The mapping between RJ45 pins and SoM generic signal names is shown below:

SoM Signal	RJ45 pin
ETH_TX1_P	1
ETH_TX1_N	2
ETH_RX1_P	3
ETH_RX1_N	6
ETH_TX2_P	4
ETH_TX2_N	5
ETH_RX2_P	7
ETH_RX2_N	8

The recommended method for the centre tap connections on the PHY side (of the magnetics) is to capacitively couple each centre tap to Ground with its own 0.1uF capacitor. The ETH_CTT signal should be left unconnected.

The LED drivers are intended to drive LEDs attached to a maximum of 3.3V
The LED drivers can provide up to 8mA

SATA

The SATA signals come directly from the i.MX6 SATA interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
SATA_RX_P	SATA_RXP
SATA_RX_N	SATA_RXN
SATA_TX_P	SATA_TXP
SATA_TX_N	SATA_TXN

These signals should be routed as differential pairs with 100R differential impedance. The signals should be ac-coupled on the host board before going to a SATA connector, using a 10nF ceramic capacitor in each line.

HDMI / DVI

The HDMI / DVI signals come from the i.MX6 HDMI interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
HDMI_C_M	HDMI_CLKM
HDMI_C_P	HDMI_CLKP
HDMI_D0_M	HDMI_D0M
HDMI_D0_P	HDMI_D0P
HDMI_D1_M	HDMI_D1M
HDMI_D1_P	HDMI_D1P
HDMI_D2_M	HDMI_D2M
HDMI_D2_P	HDMI_D2P
HDMI_HPD	HDMI_HPD
CEC	HDMI_DDCCEC

These signals should be routed as differential pairs with 100R differential impedance.

I2C bus A is suitable for use as a DDC channel as it is already at the correct level (5V).

The i.MX6 can provide compliance with HDMI V1.4a, DVI V1.0, and HDCP V1.4

PCI EXPRESS

The PCI Express signals comes from the i.MX6 PCIE interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
PCIE_CLK_P	CLK1_P
PCIE_CLK_N	CLK1_N
PCIE_TX_P	PCIE_TXP
PCIE_TX_N	PCIE_TXM
PCIE_RX_P	PCIE_RXP
PCIE_RX_N	PCIE_RXM

These signals should be routed as differential pairs with 100R differential impedance.

PCIE_RX_P, PCIE_RX_N, PCIE_CLK_P, PCIE_CLK_N should be ac-coupled on the host board using a 100nF ceramic capacitor in each line.

PCIE_TX_P, PCIE_TX_N are already ac-coupled on the RM3 using a 100nF ceramic capacitor in each line.

SDIO/SD/MMC

The SD1 interface is based on the i.MX6 processor SD1 interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
SD1_DATA0	SD1_DAT0
SD1_DATA1	SD1_DAT1
SD1_DATA2	SD1_DAT2
SD1_DATA3	SD1_DAT3
SD1_CMD	SD1_CMD
SD1_CLK	SD1_CLK
SD1_CD	GPIO_1
SD1_WP	GPIO_9

Note that SD1_CD and SD1_WP are each pulled up to 3.3V with 10K on the RM3 module.

This interface is referenced to VSD1, but always works at 3.3V logic levels. VSD1 will drop to GND briefly during a reset of the SD card, but otherwise it will be 3.3V. There is no support for 1.8V operation.

The SD2 interface is based on the i.MX6 processor SD3 interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
SD2_DATA0	SD3_DAT0
SD2_DATA1	SD3_DAT1
SD2_DATA2	SD3_DAT2
SD2_DATA3	SD3_DAT3
SD2_CMD	SD3_CMD
SD2_CLK	SD3_CLK

This interface is referenced to the 3.3V power rail and always works at 3.3V logic levels.

EXPANSION BUS

The Expansion bus is based on the i.MX6 processor EIM interface. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
EXPN_D0 to EXPN_D15	EIM_D16 to EIM_D31
EXPN_A1 to EXPN_A7	EIM_DA0 to EIM_DA6
EXPN_A11	EIM_DA10
EXPN_CE0# EXPN_CE1# EXPN_CE4#	EIM_CS0 EIM_CS1 SD2_DAT2 (configured as EIM_CS[3])
EXPN_WP#	Not implemented on i.MX6 – pulled up to 3.3V via 22K6
EXPN_WE#	EIM_RW
EXPN_RE#	EIM_OE
EXPN_ALE	Not implemented on i.MX6 – pulled down to Ground via 22K6
EXPN_READY	EIM_WAIT
EXPN_CLE	Not implemented on i.MX6 – not connected
EXPN_RESET#	Derived from SD4_DAT0 (configured as gpio2 [8])

This interface is referenced to VIO, so it works at 3.3V on RM3.

EXPN_CE4# is pulled up to the 3.3V rail with 4K7.

MISCELLANEOUS

The miscellaneous signals are based on various i.MX6 interfaces. The mapping between processor signal names and SoM generic signal names is shown below:

SoM Signal	i.MX6 Processor Signal
SYS_RESWARM#	Not directly connected to i.MX6, but used to generate a processor reset.
WAKEUP#	GPIO_0
BOOT_MODE#	BOOT_MODE0 (after inversion)
EXPN_FLASH_SEL	Not directly connected to i.MX6, but used as part of the decode to determine the boot mode
WIRELESS_PWR_EN	GPIO_2
SOM_IRQA# SOM_IRQB# SOM_IRQC# CAM_IRQ	EIM_BCLK (configured as gpio6 [31]) EIM_EB0 (configured as gpio2 [28]) EIM_EB1 (configured as gpio2 [29]) EIM_LBA (configured as gpio2 [27])

SYS_RESWARM# must be pulled up on the host board to 3.3V (ideally the standby 3.3V supply). A suitable value for the pull-up would be 10K.

BOOT_MODE# is inverted before connection to BOOT_MODE0.

EXPN_FLASH_SEL is a special signal that is pulled up to 3.3V through 10K. It can be tied to Ground on the host board in order to debug issues with booting from alternative peripherals. Normally this should be left floating on the host board.

It is recommended that all interrupts are pulled up on the host board to ensure stable levels during start-up.

[NB: Whilst the interrupt lines are typically recommended to be active low or rising-edge triggered, it is possible for software to configure them to operate in other modes if required].

DOCUMENT HISTORY

Issue:	*Date:*	*Details:*
1.0	19/6/12	Initial release
1.1	23/7/12	Additional signals defined for RM3 proposed implementation. Clarifications following review
1.2	24/7/12	Current expectations for sample products added
1.3	18/1/13	Re-allocation of DVI_HPD & CEC signals following RM3 layout update
1.4	24/1/13	Added module-specifc appendices. Renamed DVI signals to HDMI. Renamed several signals as additional GPIOs. Added USB_OTG_ID.
1.5	5/2/13	Consistency changes (signal naming/table format). Correction to use of 'EXPN_FLASH_SEL' signal for RM3 and amendments to boot mode descriptions. Updated mechanical drawing re-referencing dimensions to socket alignment spigots
1.6	20/8/13	Renamed some camera bus signals, and added information about different camera operating modes. This change corresponds to revised pin assignments on RM3 Iss. 4

REFERENCES

Ref:	*Document:*	*Details:*

End of document