RM3
System on Module
User Guide

ARM Cortex A9 System on Module

Document Reference: RM3 User Guide
Document Issue: 1.4

-

Contents

Copyright

Limitations of Liability

In no event shall Blue Chip Technology be held liable for any loss, expenses or damages of any kind whatsoever, whether direct, indirect, incidental or consequential, arising from the design or use of this product or the support materials supplied with this product. If this product proves to be defective, Blue Chip Technology is only obliged to replace or refund the purchase price at Blue Chip Technology's discretion according to their Terms and Conditions of Sale.

Trademarks

Regulatory Statements

CE
This product has been designed and assessed to meet the essential protection requirements of the European EMC Directive (2004/108/EC), the Low Voltage Directive (2006/95/EC), and the R&TTE Directive (1999/5/EC) when installed and used in conjunction with the guidelines provided within this document.

[Note that compliance with the R&TTE directive is only required for those versions of the product equipped with radio frequency interfaces].

FCC
NOTE:
FCC compliance of product versions equipped with radio frequency interfaces may require specific approval for the finished products.

WARNING:

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

Safety Warning for North America

If the power lead (cord) is not supplied with the computer, select a power lead according to your local electrical regulations. In the USA use a 'UL listed' lead. In Canada use a CSA approved or 'cUL listed' lead.

Si le cordon secteur n'est pas livré avec l'ordinateur, utiliser un cordon secteur en accord avec votre code electrique nationale. En l'Etat Unis utiliser un cordon secteur 'UL listed'. En Canada utiliser un cordon secteur certifié CSA, ou 'cUL listed'.

Manual Organisation

This manual describes in detail the RM3 Product range.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard Technical References, unless it proved to be necessary to aid in the understanding of the product. This manual needs to be read in conjunction with the Blue Chip Technology SOM Specification Guide

The manual is sectioned as follows:

Introduction;
Overviews, showing outline dimensions;
Layout, showing where the various connectors are located, and their pin-out details;
Firmware Setup
Maintenance details

We strongly recommend that you study this manual and the other guides carefully before attempting to interface with the RM3.

If you have any suggestions as to additional information to include in the User Guide or find any errors concerning this manual or any other Blue Chip technology documentation please inform us of these, by contacting our Technical Services department with the relevant details.

Introduction

The Blue Chip Technology RM3 (BCT-RM3) is based on NXP's i.MX6 Cortex A9 ARM processor and sets very high standards for integration of the processor, graphics, memory, and I/O technologies together with a unique connection system for developing your new product quickly and safely.

The RM3 is a System on Module (SOM) which follows the very successful Cortex A8 based RM2. The SOM offers the core/heart of your new product where clock speeds are extremely high, tolerances very small and termination critical. This level of technology is high and the PCB's 14 layers a testament to the complexity involved.

The BCT-RM3 is available in the following configurations:

RM3	**RM3-SOM-iMX6-1GHz-N[x]-T[x]**
Example Part Number:	**RM3-SOM-iMX6-1GHz-NQ-TE**
N[x]	Number of Cores: Quad: Q, Dual: D
T[x]	Temperature: Standard (0 to 60C): S, Extended (-40 to 85C): E

The above temperatures assume sufficient cooling of the processor, so that the heat generated is not pushed back into the PCB.

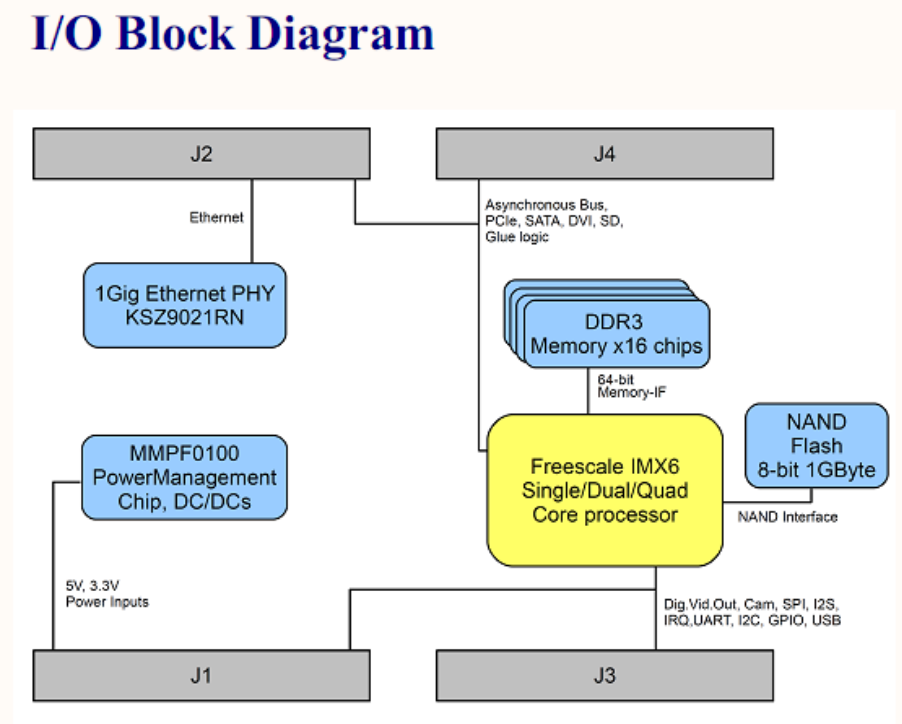
All RM3s are supplied with 1GB of SDRAM and 1GB of NAND Flash. Larger capacities are possible and subject to minimum order quantities. Alternatively, further additional NAND Flash can be added through the host board (IC, SD, MMC, CF, etc), if required.

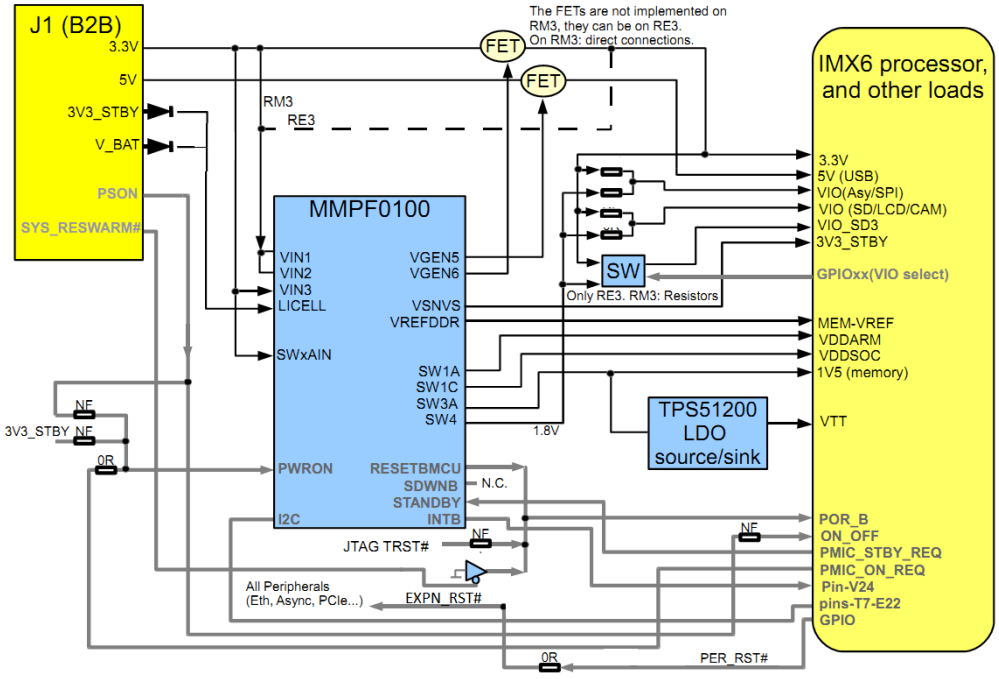
The BCT-RM3 operates from 3.3 volts and 5 volts DC. The power requirements vary depending on the CPU type and the workload. Please see the RM3 Power Requirements document for details.

To aid Hostboard development detailed schematics for reference Hostboard designs are available on request.

Functional Overview

The following block diagram shows the key components of the RM3





Specification

- NXP i.MX6 ARM Cortex-A9 1GHz Dual/Quad Core Processor with TrustZone*
- Cortex A9 NEON™ MPE (Media Processing Engine) Co-Processor per Core
- 32KB Instruction Cache + 32KB Data Cache per core
- 1 MB unified I/D L2 cache, shared by two/four cores
- 1GB 64 bit DDR3 RAM
- Hardware Accelerators
- VPU - Video Processing Unit
- IPUv3H - Image Processing Unit version 3H (2 IPUs)
- GPU3Dv4 - 3D Graphics Processing Unit (OpenGLES 2.0) version 4
- GPU2Dv2 - 2D Graphics Processing Unit (BitBlt)
- GPUVG - OpenVG 1.1 Graphics Processing Unit
- ASRC - Asynchronous Sample Rate Converter
- 1GB NAND Flash
- Integrated SATA-II interface
- 1 x SPI Bus - 2 devices
- 2 x UARTs
- 2 x I2S
- 2 x SD/MMC
- 1 x HS USB
- 1 x HS USB ULPI Bus
- 2 x I2C Bus
- 1 x OneWire Bus
- GPIO
- 10/100/1000 Ethernet
- PCI-E x1
- 1x 16 bit Asynchronous Bus (similar to X-Bus)
- 1 x Power LED
- Dual HD displays (DVI/HDMI & LCD) supported simultaneously and independently. Total raw pixel rate of all interfaces is up to 450Mpixels/sec, 24 bpp.
- One video camera/capture port - concurrent operation with dual video channels
- 1 x Mono Channel microphone input
- 1 x Mono Channel Audio output

General Precautions

Your Single Board Computer is susceptible to damage by electrostatic discharges. In order to avoid damage, you should work at an anti-static bench and observe normal anti-static precautions. Wear an anti-static wrist strap connected to an earth point *before* opening any packaging.

Where a wrist strap is not available, discharge any static charge you may have built-up by touching an earth point. Avoid any further movement that could build up another static charge. Touch an earth point from time to time to avoid further build-up, and remove the items from their anti-static bags only when required

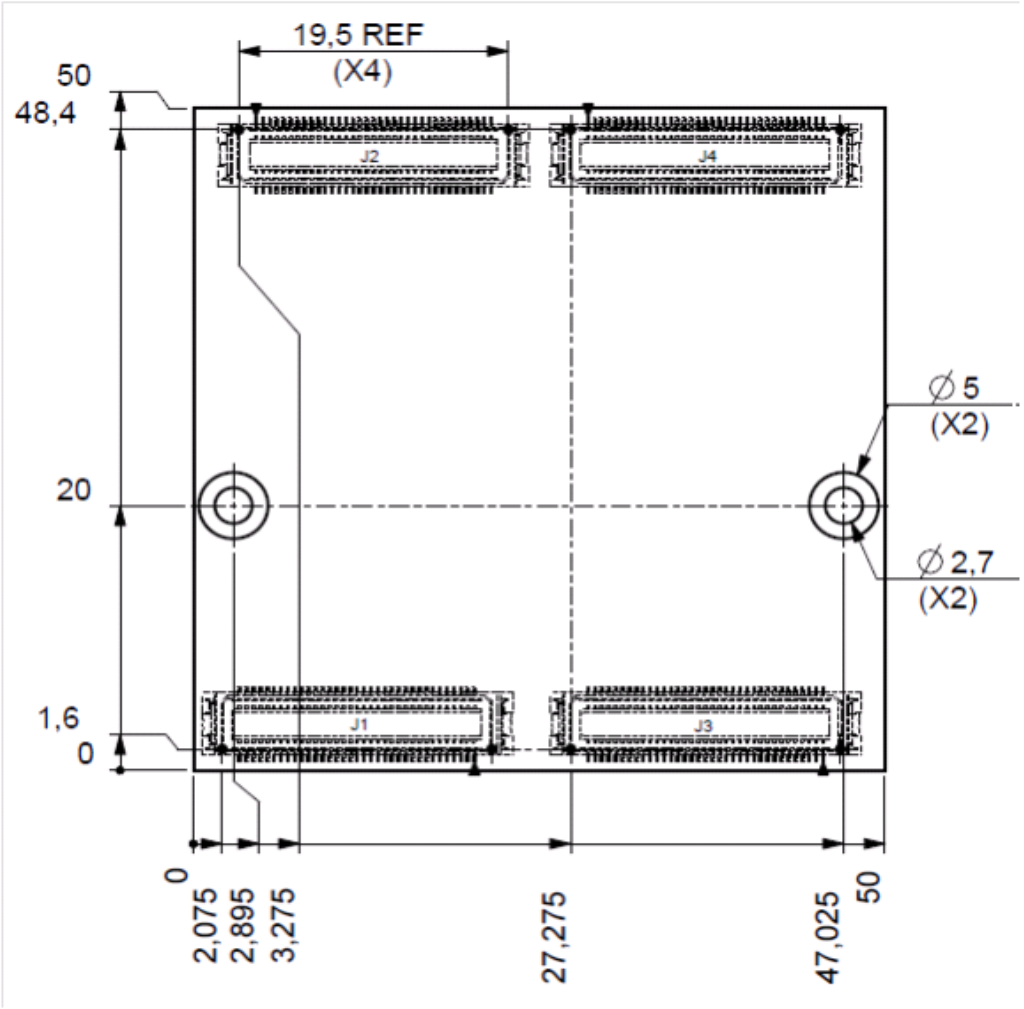
Electro-Static Discharges

If you are going to open up the unit, it is important to realise that the devices on the cards within this unit can be damaged by static electricity. Bear in mind that the damage caused by static electricity may vary from total destruction to partial damage, which may not be immediately obvious. This could have an effect on the product's reliability and warranty. Before opening the chassis, ensure that you take necessary static precautions. Ideally you should work at an anti-static bench and wear an approved wrist strap or if that is not possible, touch a suitable ground to discharge any static build up before touching the electronics. This should be repeated if the handling continues for any length of time.

If it is necessary to remove a board or electronic assembly, place it into an anti-static bag. This will prevent any static electricity build up damaging the board. Metallised bags are preferred. Do not use black anti-static bags for any item containing a battery because these tend to be conductive and will discharge the battery.

Mechanical Specifications

Outline Dimensions

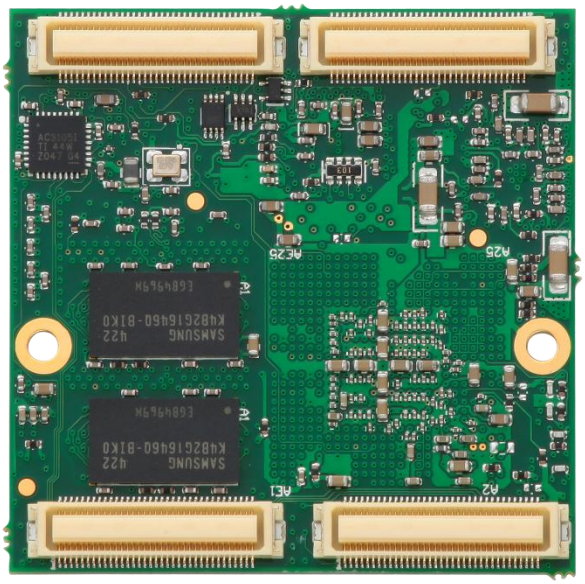


Notes:-

1. The above shows the position of the SOM mounting sockets and outline of the SOM module as seen from the top of the **PCB/host board**
2. Pin 1 position is 'rotational': it appears top-left of sockets J2 & J4 as shown, and bottom-right of sockets J1 & J3 sockets
3. Polarity is ensured by the difference in spacing of the LH & RH socket pairs: it is not possible to fit the PCB incorrectly
4. The SOM PCB should be secured in place with two mount-pillars (shown)
5. The connectors on the SOM module are 70-pin Hirose DF17-3.0-70DS-0.5 connectors. **The mating half required on the hostboard would be the Hirose DF17-XX-70DP-0.5** where XX can be 2.0 or 2.5 or 4.0 which specifies the stacking height adjustment. With the DF17-2.0-70DS-0.5 the baseboard adds 2mm to the SOM module's 3mm to create a 5mm stacking height (between PCBs). Similarly the DF17-2.5-70DS-0.5 will create a 5.5mm stacking height; the DF17-4.0-70DS-0.5 would create a 7mm stacking height. For a 5mm stack height a suitable M2.5, 5mm spacer would be Farnell p/n 1467010

N.B For thermal reasons, it is recommended that active devices are not placed beneath the module on the host/carrier board

Connector Details



In the following pin summaries, currently 'reserved' pins are greyed out. Host boards should not make connections to these pins without first consulting with Blue Chip Technology. Not all RMx SOM PCBs support all of the defined pins.

J1

LCD	LCD_ENA	2	1	GND	CAMERA
CNTRL	LCD_BL_ENA	4	3	CAM_D13	
	GND	6	5	CAM_D12	
USB	USB_HOST_P	8	7	CAM_D11	
HOST	USB_HOST_N	10	9	CAM_D10	
	GND	12	11	CAM_D9	
	USB_DEV_P	14	13	CAM_D8	
	USB_DEV_N	16	15	CAM_D7	
	GND	18	17	CAM_D6	
POWER	VCC5	20	19	GND	
	VIO	22	21	CAM_D5	
	VIO	24	23	CAM_D4	
TV	GND	26	25	CAM_D3	
	TV_LUMA_COMP	28	27	CAM_D2	
	GND	30	29	CAM_D1	
	TV_CHROMA	32	31	CAM_D0	
	GND	34	33	GND	
LCD	LCD_PWMB	36	35	CAM_STROBE	
PWM	LCD_PWMA	38	37	CAM_WEN	
	GND	40	39	CAM_FLD	
AUDIO	AUD_LINEIN_L	42	41	CAM_HS	
	AUD_LINEIN_R	44	43	CAM_VS	
	AUD_MICIN_BIAS	46	45	GND	
	AUD_MICIN_N	48	47	CAM_PCLK	
	AUD_MICIN_P	50	49	GND	
	GND	52	51	CAM_XCLKB	
	AUD_LINEOUT_R	54	53	CAM_XCLKA	
	AUD_LINEOUT_L	56	55	GND	

	GND	58	57	CAM_GLOBAL_RESET	
	IIS_DX	60	59	GND	
	IIS_DR	62	61	3V3_SBY	POWER
	IIS_CLKX	64	63	VCC3_3	
	IIS_FSX	66	65	VCC3_3	
	AUDIORSTN	68	67	VCC3_3	
	GND	70	69	VCC3_3	

J2

LAN	GND	2	1	GND	
	ETH_TX2_P	4	3	EXPN_CE0#	
	ETH_TX2_N	6	5	EXPN_CE1#	
	GND	8	7	GND	SATA
	ETH_RX2_P	10	9	SATA_RX_N	
	ETH_RX2_N	12	11	SATA_RX_P	
	GND	14	13	GND	
	ETH_TX1_P	16	15	SATA_TX_N	
	ETH_TX1_N	18	17	SATA_TX_N	
	GND	20	19	GND	DVI
	ETH_RX1_P	22	21	DVI_C_N	
	ETH_RX1_N	24	23	DVI_C_P	
	GND	26	25	GND	
	ETH_SPD_LED#	28	27	DVI_D2_N	
	ETH_LNK_LED#	30	29	DVI_D2_N	
	ETH_CTT	32	31	GND	
	GND	34	33	DVI_D1_N	
BUS	EXPN_WP#	36	35	DVI_D1_P	
EXPN	EXPN_CE4#	38	37	GND	
	EXPN_WE#	40	39	DVI_D0_N	
	EXPN_RE#	42	41	DVI_D0_P	
	EXPN_ALE	44	43	GND	
	EXPN_A11	46	45	CEC	
	EXPN_READY	48	47	DVI_HPD	
	EXPN_A7	50	49	GND	
	EXPN_A6	52	51	PCIE_CLK_P	PCIe
	EXPN_A5	54	53	PCIE_CLK_N	
	EXPN_A4	56	55	GND	
	EXPN_A3	58	57	PCIE_TX_P	
	EXPN_A2	60	59	PCIE_TX_N	
	EXPN_A1	62	61	GND	
	EXPN_D15	64	63	PCIE_RX_P	
	EXPN_D14	66	65	PCIE_RX_N	
	EXPN_D13	68	67	GND	
	GND	70	69	USB_DEV_VBUS	

J3

LCD	GND	2	1	GND	CAMERA
	LCD_D14	4	3	CAM_D14	
	LCD_D15	6	5	CAM_D15	
	GND	8	7	GND	
	LCD_D16	10	9	CAN_1	SLOW
	LCD_D17	12	11	CAN_2	SERIAL
	LCD_D18	14	13	CAN_3	
	LCD_D19	16	15	UARTA_TX	
	LCD_D20	18	17	UARTB_TX	
	LCD_D21	20	19	UARTA_ENTX	
	GND	22	21	UARTA_RX	
	LCD_D22	24	23	UARTB_RX	
	LCD_D23	26	25	GND	
	LCD_PCLK	28	27	SPI_CLK	
	GND	30	29	SPI_CSB	
	LCD_HSYNC	32	31	SPI_SIMO	
	LCD_VSYNC	34	33	SPI_SOMI	
	LCD_DE	36	35	SPI_CSA	
	LCD_D0	38	37	SOM_IRQA#	INTERRPT
	LCD_D1	40	39	SOM_IRQB#	
	LCD_D2	42	41	GND	
	LCD_D3	44	43	I2CA_SCL	I2C
	GND	46	45	I2CA_SDA	
	LCD_D4	48	47	I2CB_SCL	
	LCD_D5	50	49	I2CB_SDA	
	LCD_D6	52	51	GPIO1	GPIO
	LCD_D7	54	53	GPIO2	
	LCD_D8	56	55	GPIO3	
	LCD_D9	58	57	GPIO4	
	GND	60	59	GND	
	LCD_D10	62	61	GPIO5	
	LCD_D11	64	63	GPIO6	
	LCD_D12	66	65	GPIO7	
	LCD_D13	68	67	GPIO8	
	GND	70	69	GND	

J4

	GND	2	1	GND	
BUS	EXPN_FLASH_SEL	4	3		
EXPN	EXPN_D12	6	5		
[Continued]	EXPN_D11	8	7		
	EXPN_D10	10	9	GND	
	EXPN_D9	12	11		
	EXPN_D8	14	13		
	EXPN_D7	16	15		
	EXPN_D6	18	17		
	EXPN_D5	20	19		
	EXPN_D4	22	21	GND	
	EXPN_D3	24	23		
	EXPN_D2	26	25		
	EXPN_D1	28	27		
	EXPN_D0	30	29		
	GND	32	31		
MISC	HDQ	34	33		
	PSON	36	35		
	SYS_RES#	38	37		
	WAKEUP#	40	39	GND	
	EXPN_CLE	42	41	SD2_DATA0	SD/MMC
	BOOT_MODE#	44	43	SD2_DATA1	
	CAM_IRQ	46	45	SD2_DATA2	
	BT_PWR_EN	48	47	SD2_DATA3	
	SOM_IRQC#	50	49	SD2_CMD	
	WIRELESS_PWR_EN	52	51	SD2_CLK	
	EXPN_RESET#	54	53	GND	
	VBATT	56	55	VSD1	
	SD1_WP	58	57	SD1_SDCD	
	GND	60	59	SD1_DATA0	
		62	61	SD1_DATA1	
		64	63	SD1_DATA2	
		66	65	SD1_DATA3	
		68	67	SD1_CMD	
	GND	70	69	SD1_CLK	

Pin Definitions

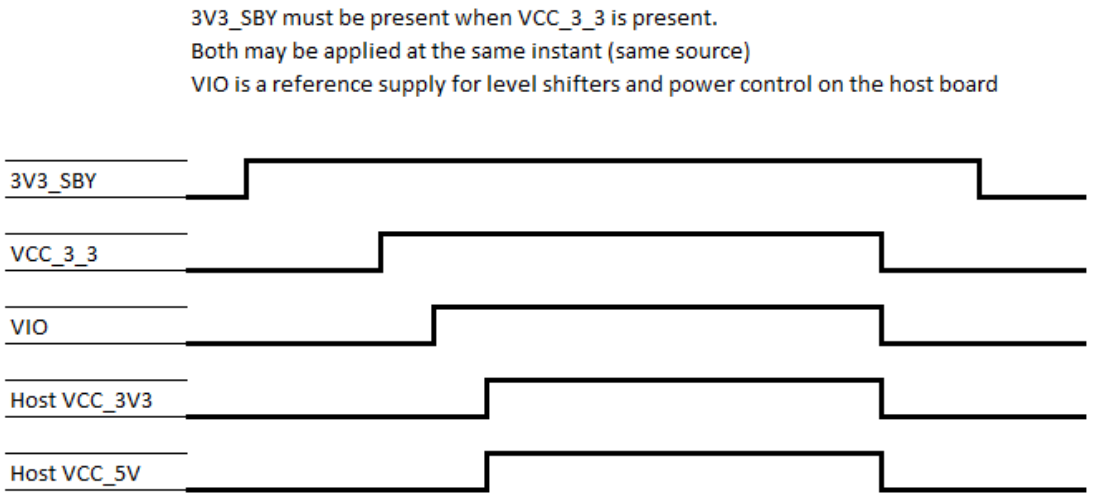
The following is an outline of some of the Signals on the SOM which relate in particular to the RM3. For a fuller list please refer to the SOM Specification Guide.

Power	***Pin Type:***	***Power Rail /Tolerance:***	***Description:***
VCC3_3	PWR	3.3V	Power feed for SOM
3V3_SBY	PWR	3.3V	Standby power feed for SOM
VIO	PWR	1.8V(typ) 3.3V (max)	Power reference from SOM
VCC5	PWR	5V	Power feed for SOM
VBATT	PWR	1.8V-3.3V	Nom 3V (1.8V-3.3V) DC power feed for SOM RTC
GND	PWR	0V	Power/signal ground

VIO is a reference supply provided by the RM3 SOM to identify the configured logic level for a number of interfaces. For flexible support of RMx SOMs, this should be used to define the SOM side of a level-shifter for affected circuits. It is possible to operate without a level-shifter if a host platform is designed for a specific RMx SOM (in which case the I/O voltage can be designed against that provided in the specific RMx documentation). The presence of VIO should be used to enable power to the peripherals on the host board in order to prevent phantom powering and failure to initialise correctly.

3V3_SBY is required, and should always be present whenever the other main supplies (VCC5 & VCC3_3) are available.

Power Sequence



Leakage voltages are prevented by use of VIO to enable power to the peripherals on the host board.
This can be achieved by enable/disable of a power supply or by a switch activated by VIO. A typical example of this is using a MIC94040 or MIC94042 for soft-start.

Power Consumption

The power consumed by RM3 varies greatly depending on what the module is doing.
For example, CPU loading affects power consumption, and so does the graphics accelerator and video accelerator.
The table below shows the current and power for various common scenarios:

Activity	Current @ 3.3V	Power
CPU idle	0.61A	2.0W
CPU 100%	0.96A	3.2W
CPU idle + VPU (video decode 800x600)	0.80A	2.6W
CPU idle + VPU (video decode 1080p)	0.85A	2.8W
CPU 100% + VPU (800x600)	1.24A	4.1W
CPU 100% + GPU (1080p) + VPU (800x600)	1.96A	6.5W

All figures are taken from a quad-core RM3 running Ubuntu 11.10 with HDMI output at 1080p@60fps and LCD output at 800x600@60fps.

Typical current for other supplies:

Power Supply	Current
3.3V Standby	< 10mA
5V	< 20mA

Provision of VBATT is optional (note that maintaining the RTC in power down may not be possible if this supply is not available). Typical drain in powered-off mode is around 7.5uA

All directions below are given with respect to the host/carrier board (ie: ‘O’ or ‘Output’ is a signal from the host board to the SOM).

LCD Interface

Digital Display #1 (Parallel/LCD)	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
LCD_D0 ....LCD_D23 LCD_HSYNC LCD_VSYNC LCD_PCLK LCD_DE	I I I I I I	VIO	24-bit parallel display interface Horizontal synchronisation Vertical synchronisation
LCD_ENA LCD_BL_ENA	I I	VIO	Enable/disable panel Enable/disable backlight

PWM Output	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
LCD_PWMA LCD_PWMB	I I	3.3V	Pulse-width modulator output Pulse-width modulator output

[If not required for brightness/contrast control, the PWM outputs can be used as general-purpose PWM outputs].

The LCD interface is designed for simple connection of panels offering a basic, parallel interface. Backlight/inverter power should be provided by the host PCB.

Slow Serial Interfaces

CAN	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
CAN_1	O	3.3V	RX (to SOM)
CAN_2	I		TX (from SOM)
CAN_3	I		TX_EN (from SOM)

The CAN transceiver is implemented on the host PCB when required.

UART A	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
UARTA_TX	I	3.3V	Serial transmit
UARTA_ENTX	I		Transmit enable control
UARTA_RX	O		Serial receive

UART B	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
UARTB_TX	I	3.3V	Serial transmit
UARTB_RX	O		Serial receive

Two, simple, two-wire UART interfaces are provided at basic logic level. UARTA adds a transmit enable signal to simplify use on multi-drop buses (eg: RS485) where disabling/tri-stating of the transceiver is required. Handshaking and access control, if desired, should be implemented at the software level (eg: using 'XON/XOFF').

UARTB is the default debug serial port. It is recommended that this be made available (as a minimum as contactable pads, or a pin header interface) on host boards.

SPI	*Host PinType:*	*Power Rail /Tolerance:*	*Description:*
SPI_CLK	I	3.3V	
SPI_CSB	I		
SPI_SIMO	I		
SPI_SOMI	O		
SPI_CSA	I		

The Serial Peripheral Interface bus provided by the SOM operates with the SOM as master, and up to two slave addresses attached (selected using SPI_CSA & SPI_CSB) operating in independent mode. Note that – if two devices are used on this bus, both must be capable of operating in multi-slave environments (ie: must support 'slave select' signalling and tri-state outputs when not addressed).

I^2C Interfaces

I^2C	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
I2CA_SCL	I/O	5V	
I2CA_SDA	I/O	5V	
I2CB_SCL	I/O	3.3V	
I2CB_SDA	I/O	3.3V	

I2CA is the default for use as a DDC channel for a display interface (see later).

GPIO

GPIO	*RMx System On Module Specification*:*	*Power Rail /Tolerance:*	*Description:*
GPIO1	I	3.3V	General purpose I/O signals
GPIO2	I		
GPIO3	I		
GPIO4	I		
GPIO5	O		
GPIO6	O		
GPIO7	O		
GPIO8	O		
GPIO9	I		
GPIO10	O		

*The direction of each GPIO interface indicated above is as defined by the RMx System On Module Specification and is supported by all RMx SOMs. The GPIO directions in the RMx System On Module Specification are defined as fixed direction, however in the case of RM3 all GPIO signals are directly attached to the i.MX6 system on chip and can be controlled as either inputs or outputs under software control.

USB

USB Device	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
USB_DEV_P/N	I/O_{BAL}		Standard balanced USB bi-directional signal data bus
USB_DEV_VBUS	A	5V	Used to determine mode (*1)
USB_OTG_ID	O	5V	Standard USB OTG ID signal

[Note *1: The 'USB_DEV_VBUS' signal on the USB device interface is fed to the SOM to indicate presence of a suitable USB 'host' on the link].

The USB Device port is a principal interface for configuration of SOM modules. It is recommended that it be made available (at least as contactable pads, or a pin header) on host boards.

The "device" port may also support OTG functionality on some modules.

USB Host #1	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
USB_HOST_P/N	I/O_{BAL}		Standard balanced USB bi-directional signal data bus

Audio

Digital Audio	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
AUDIORSTN	I	VIO	Reset signal for host audio codecs
IIS_FSX	I	VIO	Framing for output channel
IIS_CLKX	I	VIO	Transmit/receive clock
IIS_DR	O	VIO	Receive data
IIS_DX	I	VIO	Transmit data

Analogue Audio	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
AUD_LINEOUT_L	I_A	3.3V	Left & right channel analogue signals
AUD_LINEOUT_R	I_A	3.3V	
AUD_MICIN_P	O_A	3.3V	Balanced microphone analogue signal
AUD_MICIN_N	O_A	3.3V	
AUD_MICIN_BIAS	I_A	3.3V	
AUD_LINEIN_L	O_A	3.3V	Left line input (‘mono in’ for RM2)
AUD_LINEIN_R	O_A	3.3V	Right line input

RM3 supports either digital or analogue audio. Selection is under software control. The ‘AUDIORSTN’ signal will be permanently active from RM3 whilst software selection is of the on-board codec (thus holding any host-board codec in hard-reset until it is enabled to avoid possible contention on the I2C & IIS buses).

The analogue audio channel provides signal levels typically up to 0dBu (0.775V rms).

AUD_MICIN_BIAS is a configurable, low-voltage bias voltage to power suitable microphones

Video/Camera Interfaces

Digital Video In #1	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
CAM_GLOBAL_RESET	I	VIO	
CAM_PCLK	O	VIO	Pixel clock
CAM_VS	O	VIO	Vertical Sync
CAM_HS	O	VIO	Horizontal Sync
CAM_WEN	I	VIO	Enable camera function
CAM_D0 - CAM_D9	O	VIO	10-bit parallel data
CAM_XD0 - CAM_XD1	O	VIO	Function depends on module
CAM_XD2 - CAM_XD5	O	VIO	

The primary Digital Video Input #1 is designed for connection of cameras and similar devices to the SOM.

For maximum compatibility across modules it is recommended to use one of the following configurations:

- ITU-R BT.656 mode with 10-bit parallel data and embedded sync
- SYNC mode with 10-bit parallel data and separate Horizontal Sync and Vertical Sync

Other configurations are available, depending on which module is being used - see appendices for more information.

LAN/Ethernet

Ethernet	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
ETH_SPD_LED# ETH_LNK_LED# ETH_CTT ETH_TX1_P/N ETH_RX1_P/N	I I A BAL BAL	3.3V 3.3V	Open drain driver for “Speed” LED Open drain driver for “Link” LED Centre-tap connection from magnetics Transmit pair for 10/100Base-T Receive pair for 10/100Base-T
ETH_TX2_P/N ETH_RX2_P/N	BAL BAL		Extra pairs for 1000Base-T

All SOMs support a basic 10/100Base-T Ethernet configuration; some support Gigabit Ethernet.

The PHY is implemented on the SOM; magnetics and connectorisation are required on the host board

SATA

SATA	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
SATA_RX_P/N SATA_TX_P/N	O_{BAL} I_{BAL}		

DVI/HDMI

Digital Display #2 (DVI/HDMI)	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
HDMI_C_P/N HDMI_D0_P/N HDMI_D1_P/N HDMI_D2_P/N	I_{BAL} I_{BAL} I_{BAL} I_{BAL}	3.3V	DVI-I (HDMI 1.4a support may also be available) interface
HDMI_HPD	O	3.3V	Hot Plug Detect signal from attached displays
CEC	I/O	3.3V	‘Consumer Electronics Control’ channel (for HDMI implementations)

Digital display #2 offers DVI-SL, and may optionally offer HDMI interface support[1].

If a DDC channel is required, I2CA should be used.

PCIe

PCI Express (x1)	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
PCIE_CLK_P/N PCIE_TX_P/N PCIE_RX_P/N	I_{BAL} I_{BAL} O_{BAL}	3.3V	Single-channel PCI express interface with reference clock (for any devices requiring this feature)

[1] HDMI support may be subject to licensing

SDIO/SD/MMC

These ports provide connectivity to SD/MMC memory, or to SDIO devices (such as wireless modules).

SD/MMC/SDIO #1	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
SD1_WP SD1_CD SD1_DATA0 SD1_DATA1 SD1_DATA2 SD1_DATA3 SD1_CMD SD1_CLK VSD1	O O I/O I/O I/O I/O I/O I A	VSD1 3.3V VSD1 VSD1 VSD1 VSD1 VSD1 VSD1 [Note *1]	Port for connection of flash memory devices or SDIO communication devices. VSD1 is a voltage output from the SOM to define and provide the I/O power for the interface. It can be also be turned off & on by the SOM to shutdown attached devices or provide a hard reset.

Note *1: VSD1 is sourced from the SOM and provides power for SD1-connected devices and the reference voltage for any associated pull-up resistors. VSD1 is sourced from the 3.3V rail of the SOM.

SD/MMC/SDIO #2	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
SD2_DATA0 SD2_DATA1 SD2_DATA2 SD2_DATA3 SD2_CMD SD2_CLK	I/O I/O I/O I/O I/O I	3.3V	Port for connection of flash memory devices or SDIO communication devices. Note that voltage selection, card-detection, and write-protect features are not available for this interface

Key Notes for Compatibility

SD1 is primarily designed for use with SD/MMC/SDIO devices. All RMx modules support 4-bit SD/SDIO/MMC cards operating at 'higher' voltage levels (typically 2.7V to 3.6V); not all RMx modules support switching to lower voltage mode (1.7V to 1.95V), but all support power cycling to enable card reset. Mechanical 'Write Protect' is not supported by all RMx cards. RM3 **only** supports 3.3V operation.

SD2 is available for SD/MMC/SDIO type devices, but does not support any power control features or mechanical card detect/write protect. It is more appropriate for use as an interface to embedded devices on the host board.

For maximum compatibility, SD/SDIO or uSD devices are recommended.

The power supply should be decoupled at the card slot to minimise hot-insertion transients. Values of 47uF for SD cards and 100uF for SDIO cards are recommended.

Expansion Bus

Expansion Bus	*Host Pin Type:*	*Power Rail /Tolerance:*	*Description:*
EXPN_A11	I	VIO	
EXPN_A7	I		
EXPN_A6	I		
EXPN_A5	I		
EXPN_A4	I		
EXPN_A3	I		
EXPN_A2	I		
EXPN_A1	I		
EXPN_D15	I/O		16-bit wide data bus
EXPN_D14	I/O		
EXPN_D13	I/O		
EXPN_D12	I/O		
EXPN_D11	I/O		
EXPN_D10	I/O		
EXPN_D9	I/O		
EXPN_D8	I/O		
EXPN_D7	I/O		
EXPN_D6	I/O		
EXPN_D5	I/O		
EXPN_D4	I/O		
EXPN_D3	I/O		
EXPN_D2	I/O		
EXPN_D1	I/O		
EXPN_D0	I/O		
EXPN_CE0#	I		Three available chip-select signals.
EXPN_CE1#	I		Note that some RMx modules may
EXPN_CE4#	I		have restrictions on the use of these
EXPN_WE#	I		Data write strobe
EXPN_RE#	I		Data read strobe
EXPN_READY	O		
EXPN_RESET#	I		Can be used as a generic system reset

The expansion bus is provided as a flexible interface to memory-mapped host-board resources. The range available may vary dependent on RMx module in use, however there is some overlap in support.

Simple non-multiplexed devices (eg: suitably-configured FPGAs) with PSRAM/NOR flash like interfaces can be supported in order to implement specialised interface functionality.

Miscellaneous

	Host Pin Type:	*Power Rail /Tolerance:*	*Description:*	*Availability:*
PSON	*I*	*3.3V*	*Control wire from SOM* *0 = Power off* *1 = Power on*	None - no longer used
SYS_RES#	O	[Use OD driver[2]]	Reset signal into SOM 0 = Reset RMx 1 = Normal operation	RM2/RM3
WAKEUP#	O	[Use OD driver]	'Wake' signal into SOM 0 = wake from sleep state 1 = [no change in state]	RM2/RM3
BOOT_MODE#	O	3.3V	[See below]	RM2/RM3
WIRELESS_PWR_EN3V	I	3.3V	Control wire from SOM 0 = Disable WLAN 1 = Enable WLAN	RM2/RM3
SOM_IRQA# SOM_IRQB# SOM_IRQC# CAM_IRQ	O O O O	VIO	Interrupt lines to SOM. 'CAM_IRQ' is dedicated to the primary digital video input. Pull up to VIO using 10K resistors on host board	RM2/RM3 RM2/RM3 RM2/RM3 RM2/RM3
EXPN_FLASH_SEL	O	3.3V	[See below]	RM3

It is recommended that miscellaneous output pins should use open-drain drivers on the host, tolerant to 5V, in order to ensure full compatibility with all RMx modules. In practice, it is unlikely that these interfaces will be presented with more than 3.3V.

Signal:	*Description:*
BOOT_MODE#	Normal (not connected): RMx boot controlled by EXPN_FLASH_SEL. Tied to GND: Force boot from USB (serial loader)
EXPN_FLASH_SEL	[Only effective if BOOT_MODE# is not connected] This pin is reserved for Blue Chip Technology use, and customers are advised to leave the pin floating (standard boot is from on-card Flash memory)

The above signals are pulled-up on the RMx (see the relevant Appendix for details), and so do not need to be pulled high on the host board in order to set a 'high' level.

BOOT_MODE# is a dual-purpose signal intended to enable:-

- Boot from alternative interface to enable initial program/re-program of the on-SOM Flash memory
- Entry into 'engineering mode' (depending on bootloader/operating system) to enable reconfiguration of operating modes of the SOM

The former is triggered if the signal is active at power-up; the latter function is reliant on using a suitable boot-loader, and is entered dependant on a software test of the same signal some time after initial power-up.

[2] Signal is pulled up on SOM (may be to any supply between 1.8V and 5V)

Cooling

Efficient cooling is essential for long and reliable operation of any electronic equipment, and the RM3 SOM is no different. While able to operate in a local ambient up to +60˚C/+85˚C (depending on processor type and cooling solution) continued long term operation at higher temperatures will reduce the life of components and ultimately the SOM itself. Therefore it is beneficial to try and keep the local ambient as low as possible. When laying out a Hostboard design, care should be taken to avoid placing heat generating components underneath the SOM.

The +60/85˚C operation is the ambient temperature close to the RM3 SOM. If the SOM is placed in a small enclosure then this “local” ambient is likely to be higher than the room ambient outside the enclosure. When choosing or designing the enclosure, care should be taken to try and minimise the temperature rise inside the enclosure over the room ambient.

At the prototype design stage it is advisable to attach thermal probes close to the SOM and at other points inside the enclosure [for instance close to heat generating components on the Hostboard] to determine the temperature difference local to the SOM in comparison with the ambient outside the enclosure.

To aid design, there is a temperature sensor on the i.MX6 chip which can be read from the Linux shell. The sensor has a file system interface, so the temperature can be obtained by reading the relevant file

cat /sys/class/thermal/thermal_zone0/temp

The following script can be used to get a temperature reading printed once every second (press CTRL+C to stop):

while true; do cat /sys/class/thermal/thermal_zone0/temp; sleep 1; done;

Where the temperature difference is high and the expected maximum working room (or free air) ambient is also high, then additional cooling arrangements may be required to keep the local ambient close to the SOM below its maximum value. For instance this could be achieved via extra ventilation holes in the enclosure, fitment of a fan, fitment of a larger heatsink or even a combination of all 3.

System Software

Operating Systems Supported

Ubuntu 14.04 LTS

Yocto 2.1 (Krogoth)

Android 4.4.3

For Linux the RM3 is supplied with a U-Boot bootloader installed in SPI NOR Flash. Source code and demonstration Operating System images are available but it is intended that customers will develop their own image suited to their particular application. Refer to the relevant Blue Chip Technology Operating System Guide for the RM3.

Note that in order to change or adjust U-Boot settings, a Serial interface (UARTB) is required.

Maintenance

The RM3 SOM module should not require any regular maintenance.

History

Issue Level	Issue Date	Author	Amendment Details
1.0	Nov 2013	Various	1st release
1.1	June 2016	TJH	Updated to include 1GB as standard, revised part number to match the new website, OS update plus general clarifications.
1.2	July 2016	BH	Corrections made to the direction of the Expansion bus Addresses, CEx, WE,RE and RESET signals
1.3	Nov 2016	TGH	Re-corrected the Expansion bus directions; clarified SYS_RES, PSON, VSD1; added power-up sequence
1.4	July 2017	DR	Clarified directions of GPIO signals in relation to the RMx System On Module Specification

Contact Details

Blue Chip Technology Ltd.
Chowley Oak
Tattenhall
Chester
CH3 9EX
U.K.
Telephone: +44 (0)1829 772000
Facsimile: +44 (0)1829 772001

www.bluechiptechnology.com

The Support email address requires the sender to be first registered on the Support Web site at

http://support.bluechiptechnology.co.uk/

To request a Returns Authorisation number, please use the RMA portal at

Http://rma.bluechiptechnology.co.uk