PCI - DIO

RoHS Compliant
PCI Isolated Digital
Input/Output Card

User Guide

Document Reference	Product User Guide
Document Issue Level	1.2

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Introduction

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About The Manual

This manual is organised into six chapters. Each chapter covers a different aspect of using the PCI-DIO. In order to get the best results from the product, the user is urged to read all chapters, paying particular note to Chapter 2 which deals with the initial installation of the card.

Overview Provides a brief introduction to the card

Chapter 1 Presents the card's technical specification. Use this section to determine the card's suitability for a particular application

Chapter 2 Explains how to install the card in your computer.

Chapter 3 Details the connections to and from the card

Chapter 4 Gives details of the card's address mapping and internal register details allowing the user to write custom software to control the card.

Chapter 5 Electromagnetic Compatibility

Chapter 6 Shows Typical Input and Output circuitry

This manual describes the complete hardware functionality of the PCI-DIO board. All the functions may not necessarily be supported by the current release of the driver.

Overview

The PCI-DIO is a PCI-compatible half-card which provides isolated digital inputs, outputs and counter/timers.

There are 16 galvanically isolated digital inputs available on the board, which will accept up to 35 Volts RMS AC or 50 Volts peak. Each input will switch at nominally +3.5 Volts.

There are 16 open collector digital outputs which are isolated from the digital inputs and the host PC but share a common ground connection.

There are also three programmable counter/timers, the enable and clock inputs being available, isolated externally, if required , and the outputs being accessible isolated, externally and as interrupt sources. A 4 MHz crystal oscillator is available on board to allow the counter/timers to act as accurate timebases.

All Input/Output lines are available at an industry standard 50 way D-type plug connector.

One PCI interrupt line may be selectively driven by the five interrupt sources on the board, the interrupting source being readily identified by software interrogation of the on-board registers. The five interrupt sources are the three counter \timer outputs and a change of state detector on each byte of the digital inputs.

The PCI-DIO is intended to be installed with the minimum of user interaction.

The board is configured by the system BIOS and by the application drivers and no on-board links are required to select functionality.

Chapter 1

Technical Specification

Number Of Input Channels	16
Maximum input voltage	± 50 Volt DC or AC peak
Input Threshold (Vth)	2.4 Volts minimum. 4.4 Volts maximum
Input current:	2.5 mA ± 200 µA for Vth < Vin < 50 V DC + 5 µA (max) for -50 V DC < Vin < Vth
Input Bandwidth:	10kHz
Number of Output Channels:	16
Maximum ON state current:	500 mA
ON state voltage:	1.6 Volts (max) @ Iout = 350 mA
Max. board output dissipation	2.1 Watts for each group of 8 outputs (outputs 1 to 8 and 9 to 16)
Maximum OFF state voltage:	50 Volts DC
Output latency:	2.4 ms max
Maximum Isolation Voltage:	300 Volts DC or AC peak
Counters/timers:	3 x 16 Bit Counter/timers 0, 1 and 2 may be cascaded to provide a single 48 bit counter/timer. All Counter/timers may be clocked externally at a maximum rate of 10 kHz
On board Oscillator:	Frequency 4 MHz Stability ± 100ppm 0 – 70 °C
Interrupt Sources:	Register selectable to 3 counter/timer outputs and 2 input change of state detection groups
Interrupt levels supported:	All PCI interrupts
Address Overhead:	12 contiguous addresses in 12 byte block

Board Power Requirement:	2.1W This board requires both 5V and 3V3 power lines but can operate with Vio of either 3.3V or 5V
Temperature:	
Non Operating:	-20 °C to 70 °C
Operating:	0 °C to 70 °C
MTBF:	105,000 hours (Bellcore method)
Signal Connections:	1 x 50 way male “D-type” plug
Dimensions	125 (L) x 91 (H) board only 135 (L) x 122 (H) x 22 (W) including bracket

Chapter 2

Installing the PCI-DIO

The card is installed by removing the cover of the host computer and inserting the card into a free PCI slot. The rear panel of the card should then be secured to the rear panel of the host computer with the screw supplied with the computer.

When the computer is switched on, the BIOS will detect the presence of the card and will allocate it with a base address and an interrupt. These parameters may then be used to configure application software to access the card.

If the card is to be directly accessed by a user's application, it will be necessary for the application to determine where the BIOS has located the card.

One way of determining the Base address of the card can be found by using the "bc_probe" utility which is supplied on the Blue Chip Support CD, or alternatively can be downloaded from the Blue Chip website

This program must be run under DOS or a Full Screen session under Windows. It will not operate in a DOS Window.

The BC_probe utility will return addresses which look like the following

bar1, IO, 0xC800
bar2, IO, 0xC400

The Bar 1 address just sets up address space in memory to be used by the card while the Bar 2 address is the base address for the Registers for the card.

These can be used as follows in conjunction with the Address map on page x of this user manual.

Base+0 Interrupt Enable Register R/W >> 0xC400
Base+1 Interrupt Status Register R >> 0xC401
...
Base+B Counter/Timer Control Register W >> 0xC40B

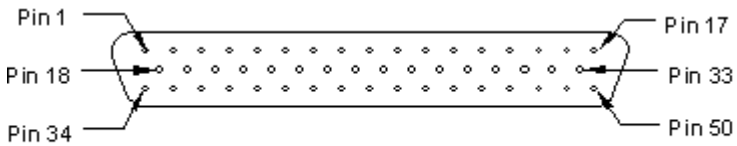
Chapter 3

Connection Details

The following table refers to the 50 way D-type plug on the rear of the card

PIN	USAGE	PIN	USAGE	PIN	USAGE
1	Digital Input 1 or counter timer 0 clock (+ve)	18	Digital Input 1 or counter timer 0 clock (-ve)	34	Digital Output 1 (+ve)
2	Digital Input 2 or counter timer 0 enable (+ve)	19	Digital Input 2 or counter timer 0 enable (-ve)	35	Digital Output 2 (+ve)
3	Digital Input 3 or counter timer 1 clock (+ve)	20	Digital Input 3 or counter timer 1 clock (-ve)	36	Digital Output 3 (+ve)
4	Digital Input 4 or counter timer 1 enable (+ve)	21	Digital Input 4 or counter timer 1 enable (-ve)	37	Digital Output 4 (+ve)
5	Digital Input 5 or counter timer 2 clock (+ve)	22	Digital Input 5 or counter timer 2 clock (-ve)	38	Digital Output 5 (+ve)
6	Digital Input 6 or counter timer 2 enable (+ve)	23	Digital Input 6 or counter timer 2 enable (-ve)	39	Digital Output 6 (+ve)
7	Data Input 7 (+ve)	24	Data Input 7 (-ve)	40	Digital Output 7 (+ve)
8	Data Input 8 (+ve)	25	Data Input 8 (-ve)	41	Digital Output 8 (+ve)
9	Data Input 9 (+ve)	26	Data Input 9 (-ve)	42	Digital Output 9 (+ve)
10	Data Input 10 (+ve)	27	Data Input 10 (-ve)	43	Digital Output 10 (+ve)
11	Data Input 11 (+ve)	28	Data Input 11 (-ve)	44	Digital Output 11 (+ve)
12	Data Input 12 (+ve)	29	Data Input 12 (-ve)	45	Digital Output 12 (+ve)
13	Data Input 13 (+ve)	30	Data Input 13 (-ve)	46	Digital Output 13 (+ve)
14	Data Input 14 (+ve)	31	Data Input 14 (-ve)	47	Digital Output 14 or counter/timer 0 out (+ve)
15	Data Input 15 (+ve)	32	Data Input 15 (-ve)	48	Digital Output 15 or counter/timer 1 out (+ve)
16	Data Input 16 (+ve)	33	Data Input 16 (-ve)	49	Digital Output 16 or counter/timer 2 out (+ve)
17	Digital Output Ground			50	Digital Output Ground

The following diagram shows how the pins on the male D-type connector are numbered



D-Type Plug, Viewon Connecting

If you are having difficulty in obtaining suitable cables to attach to the PCI-DIO, the Farnell part numbers for suitable connectors are 1084683 and 4155312.

Suitable Interface Signal Types

Each PCI-DIO digital input has two connections across which a voltage is connected. This voltage may be between -50 Volts and +50 Volts. Any voltage between -50 Volts and +2.4 Volts will be interpreted as logic zero, and any voltage between +4.4 Volts and +50 Volts will be interpreted as logic 1.

The input current for on each input signal is a constant 2.5mA, when the input conforms to the logic 1 requirements, and 5µA (max) for a logic 0.

The digital output connections are open collector with a pair of common ground connections. When energised, an output will sink up to 500mA. with a saturation voltage of 1.6Volts at 350mA. load. When de-energised, the outputs will withstand 50 Volts DC.

There is no electrical connection between the each of the input circuits, the outputs circuits and the host PC.

If an output is driving any form of inductive load, it is recommended that a reverse biased diode is connected across the load to catch back EMFs generated when the output is de-energised and the current falls to zero.

Typical input and output circuits are shown in Chapter 6.

Chapter 4

This chapter provides brief details of the cards internal registers.

Address Map

The address map for the PCI-DIO occupies a 12-byte block of addresses.

All the following addresses are relative to PCI base address register 2, located at address 18 (hex) in the PCI configuration space.

ADDRESS	FUNCTION	READ/ WRITE	Data Width
Base + 0	Interrupt enable register IER	R/W	Byte
Base + 1	Interrupt status register ISR	R	Byte
Base +2	Counter Input Select Register A CISR_A	W	Byte
Base + 3	Counter Input Select Register B CISR_B	W	Byte
Base + 4	Data Output Buffer	W	Word
Base + 6	Data Input Buffer	R	Word
Base + 8	Counter/timer 0 Count Register	R/W	Byte
Base + 9	Counter/timer 1 Count Register	R/W	Byte
Base + A	Counter/timer 2 Count Register	R/W	Byte
Base + B	Counter/timer Control Register	W	Byte

Note: For full details of the Counter/Timer Count Registers and Control Register please refer to the relevant data sheets. Presented below is a brief summary of the main features.

Digital Outputs

By writing a byte or word to the Data Output Buffer (word write to base + 4), the digital outputs may be controlled. A logic 1 written to the register causes the open collector output to turn on, and pull the output low. Consequently there is a logic inversion through the digital outputs of the card.

Bit 0 (Ls bit) of the Data Output Buffer controls Digital Output 1, and bit 15 (Ms bit) controls Digital Output 16.

It should be noted that there is a latency of 2.4 ms between writing to the output buffer and the output changing state.

Digital Inputs

When the Data Input Buffer is read Buffer (word read to base + 6), it reflects the true status of the digital inputs at the time when the read takes place.

Bit 0 (Ls bit) of the Data Input Buffer reflects the state of Digital Input 1 and bit 15 (Ms bit) reflects the state of Digital Input 16

i8254 Counter / Timer

The counter/timer circuit contains three independent 16-bit counters which may be operated in a variety of modes. There are five basic modes of operation with each mode providing a different output signal. Presented here is a brief summary of some of the modes possible by programming the counter / timer's internal registers.

All three counter/timers may be operated independently, with separate clocks and enable controls.

Counter 0, Counter 1 and Counter 2 may be connected in series. Counter 0 output to Counter 1 clock input and/or Counter 1 output to Counter 2 clock input, to allow the facility of generating very long delay periods.

The outputs from any counter/timer may be configured to generate an interrupt when going high or low, and may also be made accessible on the back panel connector.

The clock and enable inputs of the counter/timers may also be made accessible on the back panel connector.

Counter / Timer Modes

The following modes of operation exist by programming the control register within the i8254. N.B. The interrupts may be generated when the Counter/timer outputs go low or high, selected by bits in the counter control registers.

Mode 0
When programmed, the output pin will go LOW. When the counter decrements from the value loaded into the count registers to zero, the output pin will go HIGH. It will remain high until the count is re-programmed into the count registers.

Mode 1
When the count registers are programmed the output pin will be HIGH. When a LOW going signal is applied to the gate input, the count starts and the output will fall LOW, returning HIGH at the end of the count.

Mode 2
This mode operates as a frequency divider. When programmed the output pin is HIGH. When the count decrements to a value of 1 the output pin will go LOW for ONE clock cycle only and then return HIGH. This cycle repeats continuously without the need to re-program the count value.

Mode 3
When programmed the output pin will toggle each time the count register decrements to its base level from the value programmed into it. If the count value loaded is an odd number then the counter will reach zero before the output pin toggles. This mode therefore acts as a frequency divider with an approximate 1:1 mark-space ratio.

Mode 4
This mode is similar to mode 2 but the output pin pulses when the count reaches zero instead of 1.

Mode 5
This mode is similar to mode 4 except that the count sequence is triggered by the gate line.

Counter Control

The control and output lines of the counter/timer may be accessed on the rear panel connector by sacrificing some of the digital I/O lines.

The clock inputs of the i8254 counter/timer are selected using the Counter Input Select Register A at Base + 2 (Hex), as shown below:-

Counter Input Select Register A (Base + 2) CISR_A		
Bit no.	**Function**	
b7	Not Used	
b6	Counter 0 interrupt level:-	0 = Interrupt on counter out low 1 = Interrupt on counter out high
b5..b4	Counter 2 clock source:-	00 = 4 MHz clock 01 = IN5 input line 10 = Counter 1 output 11 = IN9 input line
b3..b2	Counter 1 clock source:-	00 = 4 MHz clock 01 = IN3 input line 10 = Counter 0 output 11 = IN9 input line
b1..b0	Counter 0 clock source:-	00 = 4 MHz clock 01 = IN1 input line 10 = Counter 2 output 11 = IN9 input line

The digital input bandwidth is limited such that the external clock inputs cannot be guaranteed at frequencies in excess of 10kHz. Similarly, the external enable inputs can only time external events to an accuracy of 100µS.

The enable inputs and the destination of the outputs of the i8254 counter are selected using the Counter Input Select Register B at Base + 3 (Hex), as shown in the next table

Counter Input Select Register B (Base + 3) CISR_B	
Bit no.	**Function**
b7	Counter 2 interrupt level:- 0 = Interrupt on counter out low 1 = Interrupt on counter out high
b6	Counter 1 interrupt level:- 0 = Interrupt on counter out low 1 = Interrupt on counter out high
B5	Output 16 Source 0 = Bit 15 data output buffer 1 = Counter/timer 2 output
b4	Output 15 Source 0 = Bit 14 data output buffer 1 = Counter/timer 1 output
b3	Output 14 Source 0 = Bit 13 data output buffer 1 = Counter/timer 0 output
b2	Counter 2 enable source:- 0 = Permanently enabled 1 = IN6 input line
b1	Counter 1 enable source:- 0 = Permanently enabled 1 = IN4 input line
b0	Counter 0 enable source:- 0 = Permanently enabled 1 = IN2 input line

One or more of the counter timer outputs may be made available to the user at Digital Outputs 14 to 16.

It should be noted that the 2.4 mS latency between the counter/timer output changing state and the output pin reflecting that change will still exist, so the accuracy of the output time periods generated cannot be guaranteed to be better than this delay.

Interrupt Selection

A total of five sources of interrupt are available from the digital inputs and the counter/timers. These interrupts are summarised below:-

- INT1 (COS0) is asserted whenever any of Digital Inputs 1 to 8 change state.

- INT2 (COS1) is asserted whenever any of Digital Inputs 9 to 16 change state.

- INT3 is the output from Counter/timer 0, and may be used to generate interrupts on timed events.

- INT4 is the output from Counter/timer 1, and may be used to generate interrupts on timed events.

- INT5 is the output from Counter/timer 2, and may be used to generate interrupts on timed events.

The use of interrupts is not essential but greatly enhances the functionality of the card.

To enable the generation of an interrupt or a combination of interrupts, an enable word must be written to the Interrupt Enable Register at Base + 0 (Hex), as shown below:-

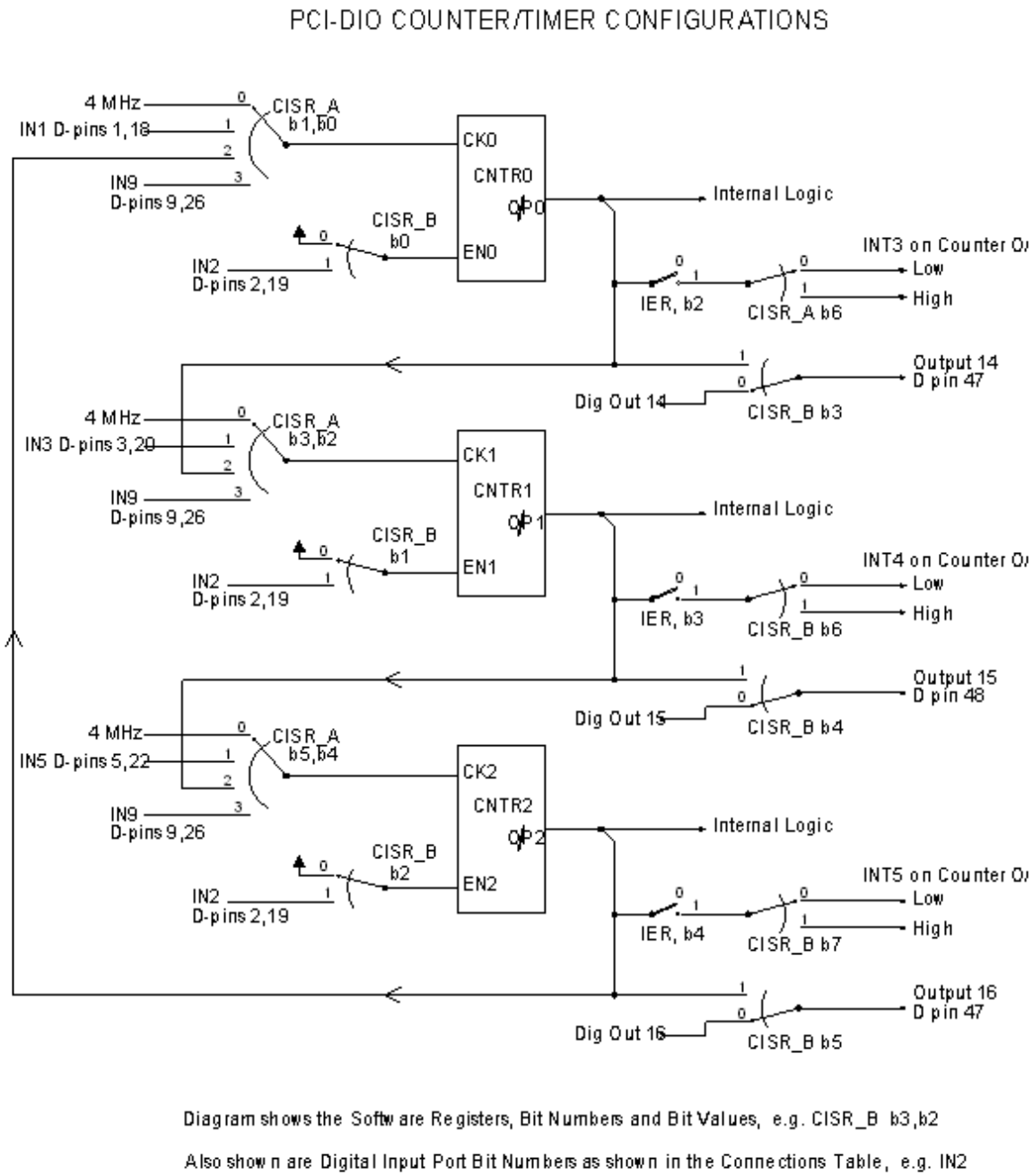
Interrupt Enable Register (Base + 0) IER		
Bit no.	**Function**	
b7	Not used	
b6	Not used	
b5	Not used	
b4	Counter/timer 2 interrupt control	(1 = Enable, 0 = Disable)
b3	Counter/timer 1 interrupt control	(1 = Enable, 0 = Disable)
b2	Counter/timer 0 interrupt control	(1 = Enable, 0 = Disable)
b1	Change of state 1 interrupt control	(1 = Enable, 0 = Disable)
b0	Change of state 0 interrupt control	(1 = Enable, 0 = Disable)

When an interrupt is recognised by the processor, the source or sources of interrupt may be read from the Interrupt status register at Base + 1 (Hex), as shown below:-

Interrupt Status Register (Base + 1) ISR	
Bit no.	**Function**
b7	Not used
b6	Not used
b5	Not used
b4	Counter/timer 2 interrupt occurred
b3	Counter/timer 1 interrupt occurred
b2	Counter/timer 0 interrupt occurred
b1	Change of state 1 interrupt occurred
b0	Change of state 1 interrupt occurred

Having serviced an interrupt, the source may be cleared by momentarily clearing the relevant bit in the interrupt enable register.

The following diagram illustrates the various interconnections of the counter/timers and the registers and bits controlling them.



Chapter 5

Electromagnetic Compatibility (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in our standard industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements of EN55022:1995 for a Class A product subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for an industrial environment.
- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.
- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.
- Most EMC problems are caused by the external cabling to boards. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple "pig-tail". Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC.
- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.
- Cables which connect externally to boards at TTL levels should not exceed two metres in length.

Failure to observe these recommendations may invalidate the EMC compliance.

> Warning
>
> This is a Class A Product. In a domestic environment this product may cause radio-interference in which case the user may be required to take adequate measures.

EMC Specification

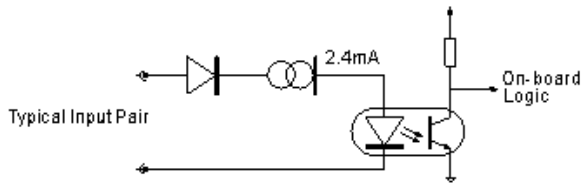
A suitably compliant industrial PC fitted with this card meets the requirements of the European Union Electromagnetic Compatibility Directive 89/336/EEC and its amending Directives, and specifically the following standards:

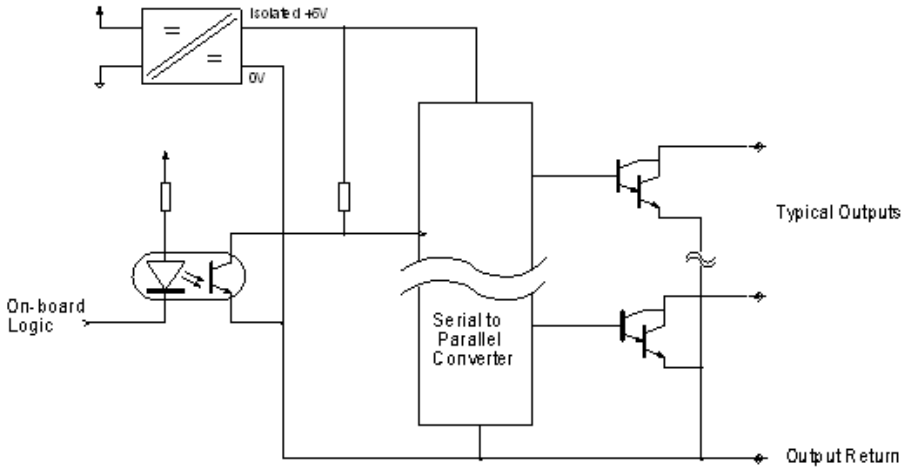
Emissions	EN 55022:1998	Class A
Immunity	EN 55024:1998	

Chapter 6

Typical Input and Output circuits

PCI-DIO Input / Output Circuitry





Amendment History

Issue Level	Issue Date	Author	Amendment Details
1.0	15/01/2007	TMCK	Initial Release
1.1	07/02/2007	TMCK	Added MTBF figures, corrected EMC details and grammar changes
1.2	21/03/2007	TMCK	Corrected drawings which were reversed

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