

## PCl-ADC data anustion card

The PCI-ADC is a PCI-compatible halfcard which provides analogue and digital input/outputs and counter/timers. Eight differential or sixteen single ended analogue inputs are available with 12-bit resolution and programmable gain to allow full scale input ranges of between $\pm 5 \mathrm{mV}$ and $\pm 5$ volts. The maximum sample rate of these is $230 \mathrm{KS} / \mathrm{s}$.

A FIFO input buffer is available such that 1024 analogue samples may be taken before processor intervention is required. Four bipolar analogue outputs are provided to 12 bits resolution. Each may be individually configured as voltage or current outputs with full scale range of $\pm 10$ volts or $\pm 20 \mathrm{~mA}$.

There are 24 TTL-compatible programmable digital input/outputs available from the board and there are also three programmable counter/timers, the outputs of which may be used to generate interrupts, to initiate analogue input conversion, analogue output sample update, or digital I/O. A 4 MHz crystal oscillator is available on board to allow the counter/timers to provide accurate timebases.

OPTIONS


1 metre cable with IDC and D type connector (P/N 1371 0071)

50 way screw terminal adapter (P/N 1981-0004)


- Windows® 98/2000, NT® and $\mathrm{XP®}$ drivers
$\underset{\text { Solution Provider }}{\text { AMD }}$
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## TECHNICAL SPECIFICATION

## Analogue Inputs

- 6 single ended inputs or 8 differential input
- Range of $\pm 5$ Volts maximum operating
- 12 bits resolution
- 1, 10, 100 or 1000, software selectable gain settings
- Gain accuracy - all gains without auto-cal. $= \pm 0.3 \%$. All gains with auto-cal. $= \pm 0.05 \%$
- Input offset accuracy:

Gain = 1 or 10 without auto-cal. $= \pm 0.1 \%$
Gain $=1$ or 10 with auto-cal. $= \pm 0.05 \%$
Gain $=100$ without auto-cal. $= \pm 0.2 \%$
Gain $=100$ with auto-cal. $= \pm 0.05 \%$
Gain $=1000$ without auto-cal. $= \pm 1.2 \%$

- Maximum sample rate Gain $=1000$ with auto-cal. $=$ $\pm 0.05$ \%
- Input settling time $-230 \mathrm{Ks} / \mathrm{s}$ burst, $4.3 \mu \mathrm{~s}$ conversion time
Gain $=123 \mu \mathrm{~s}$ all typical to $0.1 \%$
Gain $=1024 \mu \mathrm{~s}$
Gain $=100100 \mu \mathrm{~s}$
- Data buffer gain = $10001000 \mu \mathrm{~s}$, FIFO 16 bits wide $\times 1024$ samples, with channel number identification on each sample


## Analogue Outputs

- 4 outputs
- 12 bits output resolution
- Constant voltage or constant current formats, individually software selectable
- Output levels -

Voltage mode $= \pm 10$ volts
Current mode $= \pm 20 \mathrm{~mA}$

- Drive capability

Voltage mode $= \pm 20 \mathrm{~mA}$ (FS into 500R min.)
Current mode $= \pm 12$ volts (FS into 600R max.)

- Accuracy

Voltage mode $= \pm 0.15 \%$
Current mode $= \pm 3.5 \%$

## Interrupls

- Interrupt sources:

Register selectable to 3 Counter/timer outputs, 2 PIO handshake control lines, ADC busy and FIFO Not Empty/Half full.

- All PCI interrupt levels supported
- Address overhead of 26 I/O addresses in 3 PCl address spaces


## Digital Input/Output

- 24 I/O channels arranged as $3 \times 8$ I/O bits
- Signal levels at 5 Volt TTL Logic
- Output

Logic Low Level: 0 V (min) - 0.4V (max) @ $\mathrm{IOL}=2.5 \mathrm{~mA}$
Logic High Level: 3.5V (min) - 5V (max) @ $\mathrm{IOH}=-400 \mathrm{~mA}$

- Drive Current 2.5 mA (Logic Low) Vout $=0.4$ Volts -400 mA (Logic High) Vout $=3.5$ Volts
- $\pm 10 \mathrm{~mA}$ Input Loading
- Terminator resistor packs are fitted to each I/O port to pull the lines to +5 volts. Optionally they may pull the lines down to 0 volts.


## Counter/Timers

- $3 \times 16$ Bit Counter/timers. may be cascaded.
- Onboard oscillator -4 MHz frequency, stability $\pm$ 100ppm $0-70^{\circ} \mathrm{C}$


## Mechanicals

- Signal Connections - $1 \times 50$ way male ' $D$-type' plug
- Dimensions - $165(\mathrm{~L}) \times 100(\mathrm{H})$ board only, $180(\mathrm{~L}) \times 122(\mathrm{H}) \times 22(\mathrm{~W})$ including bracket


## Power

- +3.3 Volts, 0.5 W max and +5 Volts, 1.2 W max

